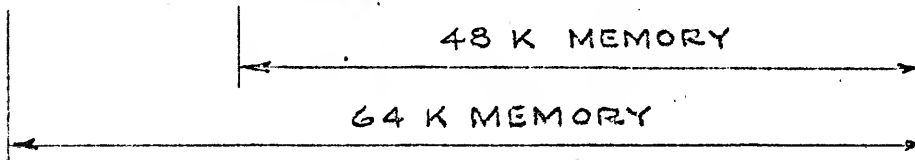


# P.C. ALTO CARD ARRANGEMENT

CARD SLOT	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1				
	5	12	5	12	5	12	5	12	5	12	5	12	5	12	5	12	* MEMORY	*	* MEMORY	MEMORY INTERFACE	ARITHMETIC CARD	CONTROL CARD	* RAM CONTROL STORE	DISPLAY CONTROL	DISK CONTROL	* ETHERNET	* PROC BUS DEVICE	* PROC BUS DEVICE				
CARD NAME	B I T															B I T																
M E M O R Y																																



\* OPTIONAL CARD  
NOT PART OF  
BASIC ALTO.

\* FILE CREATED 1-FEB-77 11:45:39  
 \* ALTOBP NL MAIN WIRELIST

\$\$ +:								0	\$
+15V:	1*7	2*7	3*7					0	1
-15V:	1*8	2*8	3*8					0	2
-5ACT:	7*102							0	3
-6ACT:	7*101							0	4
ALUF0:	7*40	8*40						0	5
ALUF1:	7*41	8*41						0	6
ALUF2:	7*42	8*42						0	7
ALUF3:	7*43	8*43						0	8
ALU[00]:	6*100	8*100	9*100					0	9
ALU[01]:	6*101	8*101	9*101					0	10
ALU[02]:	6*102	8*102	9*102					0	11
ALU[03]:	6*103	8*103	9*103					0	12
ALU[04]:	6*104	8*104	9*104					0	13
ALU[05]:	6*105	8*105	9*105					0	14
ALU[06]:	6*106	8*106	9*106					0	15
ALU[07]:	6*107	8*107	9*107					0	16
ALU[08]:	6*108	8*108	9*108					0	17
ALU[09]:	6*109	8*109	9*109					0	18
ALU[10]:	6*110	8*110	9*110					0	19
ALU[11]:	6*111	8*111	9*111					0	20
ALU[12]:	6*112	8*112	9*112					0	21
ALU[13]:	6*113	8*113	9*113					0	22
ALU[14]:	6*114	8*114	9*114					0	23
ALU[15]:	6*115	8*115	9*115					0	24
AUSYSCLK:	3*72	5*72	8*72					0	25
-AUSYSCLK:	3*12	4*75	5*8	7*70	8*8			0	26
-BLOCK:	4*110	5*110	7*110					0	27
BS0:	7*120	9*120						0	28
BS1:	7*121	9*121						0	29
BS2:	7*122	9*122						0	30
BSZ0:	7*44	8*44						0	31
BUS[00]:	1*80	2*80 8*80	3*80 9*80	4*80	5*80	6*80	7*80	0	32
BUS[01]:	1*81	2*81 8*81	3*81 9*81	4*81	5*81	6*81	7*81	0	33
BUS[02]:	1*82	2*82 8*82	3*82 9*82	4*82	5*82	6*82	7*82	0	34

BUS[03]:	1*83	2*83 8*83	3*83 9*83	4*83	5*83	6*83	7*83	0	35
BUS[04]:	1*84	2*84 8*84	3*84 9*84	4*84	5*84	6*84	7*84	0	36
BUS[05]:	1*85	2*85 8*85	3*85 9*85	4*85	5*85	6*85	7*85	0	37
BUS[06]:	1*86	2*86 8*86	3*86 9*86	4*86	5*86	6*86	7*86	0	38
BUS[07]:	1*87	2*87 8*87	3*87 9*87	4*87	5*87	6*87	7*87	0	39
BUS[08]:	1*88	2*88 8*88	3*88 9*88	4*88	5*88	6*88	7*88	0	40
BUS[09]:	1*89	2*89 8*89	3*89 9*89	4*89	5*89	6*89	7*89	0	41
BUS[10]:	1*90	2*90 8*90	3*90 9*90	4*90	5*90	6*90	7*90	0	42
BUS[11]:	1*91	2*91 8*91	3*91 9*91	4*91	5*91	6*91	7*91	0	43
BUS[12]:	1*92	2*92 8*92	3*92 9*92	4*92	5*92	6*92	7*92	0	44
BUS[13]:	1*93	2*93 8*93	3*93 9*93	4*93	5*93	6*93	7*93	0	45
BUS[14]:	1*94	2*94 8*94	3*94 9*94	4*94	5*94	6*94	7*94	0	46
BUS[15]:	1*95	2*95 8*95	3*95 9*95	4*95	5*95	6*95	7*95	0	47
CARRY:	8*73							0	48
-CE:	9*14	13*75 19*75 25*75	14*75 20*75 26*75	15*75 21*75 27*75	16*75 22*75 28*75	17*75 23*75	18*75 24*75	0	49
-CONST+:	6*97	7*97	9*97					0	50
-CS0:	9*15	13*76	14*76	15*76	16*76			0	51
-CS1:	9*75	17*76	18*76	19*76	20*76			0	52
-CS2:	9*76	21*76	22*76	23*76	24*76			0	53
-CS3:	9*77	25*76	26*76	27*76	28*76			0	54
CSYSCLK:	5*70							0	55
-CURTAC:	5*114	7*114						0	56
DBARC:	1*63	2*63	3*63	5*63	6*63	7*63		0	57
DBSYSCLK:	5*62	6*62	7*62					0	58
DCLK:	5*10							0	59
DDR+:	5*6	7*6						0	60
-DHTAC:	5*23	7*23						0	61
DNS:	7*75	8*75						0	62
-DS0:	9*19	13*79 25*79	14*79 26*79	17*79	18*79	21*79	22*79	0	63
-DS1:	9*18	15*79 27*79	16*79 28*79	19*79	20*79	23*79	24*79	0	64
-DVTAC:	5*22	7*22						0	65

170ns

1.2µs

-DWTAC:	5*24	7*24					0	66
EMACT:	3*99	6*99	7*99	8*99			0	67
-ETAC:	3*100	7*100					0	68
F1[0]:	1*30	2*30	3*30	4*30	7*30		0	69
F1[1]:	1*31	2*31	3*31	4*31	7*31		0	70
F1[2]:	1*32	2*32	3*32	4*32	7*32		0	71
F1[3]:	1*33	2*33	3*33	4*33	7*33		0	72
-F2EQ10:	5*51	7*51					0	73
-F2EQ11:	5*116	7*116	8*116				0	74
F2[0]:	1*36	2*36	3*36	4*36	7*36	8*36	0	75
F2[1]:	1*37	2*37	3*37	4*37	7*37	8*37	0	76
F2[2]:	1*38	2*38	3*38	4*38	7*38	8*38	0	77
F2[3]:	1*39	2*39	3*39	4*39	7*39		0	78
IBUSY:	3*113						0	79
-IR[00]:	7*10	8*10					0	80
-IR[01]:	7*11	7*12	8*11	8*12			0	81
-IR[03]:	7*13	8*13					0	82
-IR[04]:	7*14	8*14					0	83
-IR[05]:	7*15	8*15					0	84
-IR[06]:	7*16	8*16					0	85
-IR[07]:	7*78	8*78					0	86
-IR[08]:	7*18	8*18					0	87
-IR[09]:	7*19	8*19					0	88
-IR[10]:	8*20						0	89
-IR[11]:	8*21						0	90
-IR[12]:	8*22	8*23					0	91
-IR[14]:	8*24						0	92
-IR[15]:	8*25						0	93
IR+:	7*71	8*71					0	94
-KSTAC:	4*28	7*28					0	95
KSYSCLK:	4*7	5*7					0	96
-KWDTAC:	4*25	7*25					0	97
LALUC0:	7*49	8*49					0	98
-LCY8:	7*48	8*48					0	99
LOADL:	7*7	8*7					0	100
LOADR:	7*68	8*68					0	101
-LOADT:	7*69	8*69					0	102
-LSH1:	7*46	8*46					0	103
MAR[05]:	9*40	13*101	14*101	15*101	16*101	17*101	18*101	
		19*101	20*101	21*101	22*101	23*101	24*101	
		25*101	26*101	27*101	28*101			0 104

MAR[06]:	9*39	13*100 19*100 25*100	14*100 20*100 26*100	15*100 21*100 27*100	16*100 22*100 28*100	17*100 23*100	18*100 24*100	0	105
MAR[07]:	9*41	10*41 16*102 22*102 28*102	11*41 17*102 23*102	12*41 18*102 24*102	13*102 19*102 25*102	14*102 20*102 26*102	15*102 21*102 27*102	0	106
MAR[08]:	9*42	10*42 16*103 22*103 28*103	11*42 17*103 23*103	12*42 18*103 24*103	13*103 19*103 25*103	14*103 20*103 26*103	15*103 21*103 27*103	0	107
MAR[09]:	9*50	10*50 16*111 22*111 28*111	11*50 17*111 23*111	12*50 18*111 24*111	13*111 19*111 25*111	14*111 20*111 26*111	15*111 21*111 27*111	0	108
MAR[10]:	9*52	10*52 16*113 22*113 28*113	11*52 17*113 23*113	12*52 18*113 24*113	13*113 19*113 25*113	14*113 20*113 26*113	15*113 21*113 27*113	0	109
MAR[11]:	9*44	10*44 16*105 22*105 28*105	11*44 17*105 23*105	12*44 18*105 24*105	13*105 19*105 25*105	14*105 20*105 26*105	15*105 21*105 27*105	0	110
MAR[12]:	9*51	10*51 16*112 22*112 28*112	11*51 17*112 23*112	12*51 18*112 24*112	13*112 19*112 25*112	14*112 20*112 26*112	15*112 21*112 27*112	0	111
MAR[13]:	9*46	10*46 16*106 22*106 28*106	11*46 17*106 23*106	12*46 18*106 24*106	13*106 19*106 25*106	14*106 20*106 26*106	15*106 21*106 27*106	0	112
MAR[14]:	9*43	10*43 16*104 22*104 28*104	11*43 17*104 23*104	12*43 18*104 24*104	13*104 19*104 25*104	14*104 20*104 26*104	15*104 21*104 27*104	0	113
MAR+:	7*72	9*72						0	114
-MD[00]:	9*20	10*20 15*85 21*85 27*85	11*20 17*81 23*81	12*20 17*85 23*85	13*81 19*81 25*81	13*85 19*85 25*85	15*81 21*81 27*81	0	115
-MD[01]:	9*21	10*21 15*84 21*84 27*84	11*21 17*82 23*82	12*21 17*84 23*84	13*82 19*82 25*82	13*84 19*84 25*84	15*82 21*82 27*82	0	116
-MD[02]:	9*22	10*22 15*86 21*86 27*86	11*22 17*80 23*80	12*22 17*86 23*86	13*80 19*80 25*80	13*86 19*86 25*86	15*80 21*80 27*80	0	117
-MD[03]:	9*23	10*23 15*87 21*87 27*87	11*23 17*83 23*83	12*23 17*87 23*87	13*83 19*83 25*83	13*87 19*87 25*87	15*83 21*83 27*83	0	118
-MD[04]:	9*24	10*24 15*90 21*90 27*90	11*24 17*88 23*88	12*24 17*90 23*90	13*88 19*88 25*88	13*90 19*90 25*90	15*88 21*88 27*88	0	119
-MD[05]:	9*25	10*25 15*91 21*91 27*91	11*25 17*89 23*89	12*25 17*91 23*91	13*89 19*89 25*89	13*91 19*91 25*91	15*89 21*89 27*89	0	120

-MD[06]:	9*26	10*26 15*94 21*94 27*94	11*26 17*93 23*93	12*26 17*94 23*94	13*93 19*93 25*93	13*94 19*94 25*94	15*93 21*93 27*93	0	121
-MD[07]:	9*28	10*28 15*95 21*95 27*95	11*28 17*92 23*92	12*28 17*95 23*95	13*92 19*92 25*92	13*95 19*95 25*95	15*92 21*92 27*92	0	122
-MD[08]:	9*29	10*29 15*107 21*107 27*107	11*29 17*96 23*96	12*29 17*107 23*107	13*96 19*96 25*96	13*107 19*107 25*107	15*96 21*96 27*96	0	123
-MD[09]:	9*30	10*30 15*108 21*108 27*108	11*30 17*97 23*97	12*30 17*108 23*108	13*97 19*97 25*97	13*108 19*108 25*108	15*97 21*97 27*97	0	124
-MD[10]:	9*31	10*31 15*109 21*109 27*109	11*31 17*98 23*98	12*31 17*109 23*109	13*98 19*98 25*98	13*109 19*109 25*109	15*98 21*98 27*98	0	125
-MD[11]:	9*32	10*32 15*110 21*110 27*110	11*32 17*99 23*99	12*32 17*110 23*110	13*99 19*99 25*99	13*110 19*110 25*110	15*99 21*99 27*99	0	126
-MD[12]:	9*33	10*33 16*95 22*95 28*95	11*33 18*92 24*92	12*33 18*95 24*95	14*92 20*92 26*92	14*95 20*95 26*95	16*92 22*92 28*92	0	127
-MD[13]:	9*34	10*34 16*107 22*107 28*107	11*34 18*96 24*96	12*34 18*107 24*107	14*96 20*96 26*96	14*107 20*107 26*107	16*96 22*96 28*96	0	128
-MD[14]:	9*36	10*36 16*108 22*108 28*108	11*36 18*97 24*97	12*36 18*108 24*108	14*97 20*97 26*97	14*108 20*108 26*108	16*97 22*97 28*97	0	129
-MD[15]:	9*37	10*37 16*109 22*109 28*109	11*37 18*98 24*98	12*37 18*109 24*109	14*98 20*98 26*98	14*109 20*109 26*109	16*98 22*98 28*98	0	130
MIARC:	5*71	9*71	10*71	11*71	12*71			0	131
MISYSCLK:	5*69	9*69	10*69	11*69	12*69			0	132
-NEXT[05]:	1*105	2*105	4*105	7*105				0	133
-NEXT[06]:	1*106	2*106	3*106	4*106	7*106			0	134
-NEXT[07]:	1*107	2*107	3*107	4*107	7*107			0	135
-NEXT[08]:	1*108	2*108	4*108	7*108				0	136
-NEXT[09]:	1*109	2*109	4*109	5*109	7*109			0	137
OBUSY:	3*114							0	138
OKTORUN:	1*1	2*1	3*1	4*1	6*1			0	139
-PARTAC:	7*61	9*61						0	140
-PC:	9*13	13*74 19*74 25*74	14*74 20*74 26*74	15*74 21*74 27*74	16*74 22*74 28*74	17*74 23*74	18*74 24*74	0	141
-READMOUS:	7*117	9*117						0	142
READPAR:	9*38	14*99 26*99	16*99 28*99	18*99	20*99	22*99	24*99	0	143

RESET:	1*2	2*2	3*2	4*2	6*2	7*2	9*2	0	144
RS0:	9*16	13*77	14*77	15*77	16*77	17*77	18*77		
		19*77	20*77	21*77	22*77	23*77	24*77		
		25*77	26*77	27*77	28*77			0	145
RS1:	9*12	13*73	14*73	15*73	16*73	17*73	18*73		
		19*73	20*73	21*73	22*73	23*73	24*73		
		25*73	26*73	27*73	28*73			0	146
RS2:	9*10	13*71	14*71	15*71	16*71	17*71	18*71		
		19*71	20*71	21*71	22*71	23*71	24*71		
		25*71	26*71	27*71	28*71			0	147
RS3:	9*70	13*70	14*70	15*70	16*70	17*70	18*70		
		19*70	20*70	21*70	22*70	23*70	24*70		
		25*70	26*70	27*70	28*70			0	148
RS4:	9*8	13*69	14*69	15*69	16*69	17*69	18*69		
		19*69	20*69	21*69	22*69	23*69	24*69		
		25*69	26*69	27*69	28*69			0	149
RS5:	9*11	13*72	14*72	15*72	16*72	17*72	18*72		
		19*72	20*72	21*72	22*72	23*72	24*72		
		25*72	26*72	27*72	28*72			0	150
RS6:	9*7	13*68	14*68	15*68	16*68	17*68	18*68		
		19*68	20*68	21*68	22*68	23*68	24*68		
		25*68	26*68	27*68	28*68			0	151
RS7:	9*6	13*67	14*67	15*67	16*67	17*67	18*67		
		19*67	20*67	21*67	22*67	23*67	24*67		
		25*67	26*67	27*67	28*67			0	152
RSEL0:	7*54	8*54	9*54					0	153
RSEL1:	7*55	8*55	9*55					0	154
RSEL2:	7*56	8*56	9*56					0	155
RSEL3:	7*57	8*57	9*57					0	156
RSEL4:	7*59	8*59	9*59					0	157
-RSH1:	7*47	8*47						0	158
-RSN:	3*42							0	159
SELR37:	7*74	9*74						0	160
SHZERO:	7*26	8*26						0	161
SH[00]:	7*50	8*50						0	162
-SIO:	3*41							0	163
SKIP:	8*74							0	164
SN[00]:	3*18							0	165
SN[01]:	3*19							0	166
SN[02]:	3*20							0	167
SN[03]:	3*21							0	168
SN[04]:	3*22							0	169
SN[05]:	3*23							0	170
SN[06]:	3*24							0	171
SN[07]:	3*25							0	172
-SRESET:	1*62	2*62	3*62	4*62	7*1	9*62		0	173
-STOP:	5*1	9*1						0	174
STOPCLK:	5*20	7*20						0	175

-STORE:	7*73	9*73						0	176
-SWAKMRT:	3*68	5*68	9*68					0	177
-W0:	9*79	13*78 25*78	14*78 26*78	17*78	18*78	21*78	22*78	0	178
-W1:	9*78	15*78 27*78	16*78 28*78	19*78	20*78	23*78	24*78	0	179
-WAKE5:	7*60							0	180
-WAKE6:	7*104							0	181
WAKECURT:	5*115	7*115						0	182
-WAKEDHT:	5*77	7*77						0	183
-WAKEDVT:	5*76	7*76						0	184
-WAKEDWT:	5*21	7*21						0	185
-WAKEET:	3*103	7*103						0	186
-WAKEKST:	4*8	7*8						0	187
-WAKEKWD:	4*79	7*79						0	188
-WAKEMRT:	7*67	9*67						0	189
-WAKEPART:	7*118	9*118						0	190
WRITEPAR:	9*49	14*110 26*110	16*110 28*110	18*110	20*110	22*110	24*110	0	191
XIOREF:	9*48	10*48	11*48	12*48				0	192
XMAR[15]:	9*47	10*47	11*47	12*47				0	193
XMT2:	9*98	10*98	11*98	12*98				0	194
-ZEROBUS:	7*34	8*34						0	195
+DISP:	7*98	8*98						0	196
-+KDATA:	3*111	4*111	7*111					0	197
-+KSTAT:	4*112	7*112						0	198
-+MD:	7*96	9*96						0	199

\* This card uses 1058 wires

↑L



1*1	OKTORUN	1*2	RESET	1*7	+15V	1*8	-15V
1*30	F1[0]	1*31	F1[1]	1*32	F1[2]	1*33	F1[3]
1*36	F2[0]	1*37	F2[1]	1*38	F2[2]	1*39	F2[3]
1*62	-SRESET	1*63	DBARC	1*80	BUS[00]	1*81	BUS[01]
1*82	BUS[02]	1*83	BUS[03]	1*84	BUS[04]	1*85	BUS[05]
1*86	BUS[06]	1*87	BUS[07]	1*88	BUS[08]	1*89	BUS[09]
1*90	BUS[10]	1*91	BUS[11]	1*92	BUS[12]	1*93	BUS[13]
1*94	BUS[14]	1*95	BUS[15]	1*105	-NEXT[05]	1*106	-NEXT[06]
1*107	-NEXT[07]	1*108	-NEXT[08]	1*109	-NEXT[09]	2*1	OKTORUN
2*2	RESET	2*7	+15V	2*8	-15V	2*30	F1[0]
2*31	F1[1]	2*32	F1[2]	2*33	F1[3]	2*36	F2[0]
2*37	F2[1]	2*38	F2[2]	2*39	F2[3]	2*62	-SRESET
2*63	DBARC	2*80	BUS[00]	2*81	BUS[01]	2*82	BUS[02]
2*83	BUS[03]	2*84	BUS[04]	2*85	BUS[05]	2*86	BUS[06]
2*87	BUS[07]	2*88	BUS[08]	2*89	BUS[09]	2*90	BUS[10]
2*91	BUS[11]	2*92	BUS[12]	2*93	BUS[13]	2*94	BUS[14]
2*95	BUS[15]	2*105	-NEXT[05]	2*106	-NEXT[06]	2*107	-NEXT[07]
2*108	-NEXT[08]	2*109	-NEXT[09]	3*1	OKTORUN	3*2	RESET
3*7	+15V	3*8	-15V	3*12	-AUSYSCLK	3*18	SN[00]
3*19	SN[01]	3*20	SN[02]	3*21	SN[03]	3*22	SN[04]
3*23	SN[05]	3*24	SN[06]	3*25	SN[07]	3*30	F1[0]
3*31	F1[1]	3*32	F1[2]	3*33	F1[3]	3*36	F2[0]
3*37	F2[1]	3*38	F2[2]	3*39	F2[3]	3*41	-SIO
3*42	-RSN	3*62	-SRESET	3*63	DBARC	3*68	-SWAKMRT
3*72	AUSYSCLK	3*80	BUS[00]	3*81	BUS[01]	3*82	BUS[02]
3*83	BUS[03]	3*84	BUS[04]	3*85	BUS[05]	3*86	BUS[06]
3*87	BUS[07]	3*88	BUS[08]	3*89	BUS[09]	3*90	BUS[10]
3*91	BUS[11]	3*92	BUS[12]	3*93	BUS[13]	3*94	BUS[14]
3*95	BUS[15]	3*99	EMACT	3*100	-ETAC	3*103	-WAKEET
3*106	-NEXT[06]	3*107	-NEXT[07]	3*111	-KDATA	3*113	IBUSY
3*114	OBUSY	4*1	OKTORUN	4*2	RESET	4*7	KSYSCLK
4*8	-WAKEKST	4*25	-KWDTAC	4*28	-KSTAC	4*30	F1[0]
4*31	F1[1]	4*32	F1[2]	4*33	F1[3]	4*36	F2[0]
4*37	F2[1]	4*38	F2[2]	4*39	F2[3]	4*62	-SRESET
4*75	-AUSYSCLK	4*79	-WAKEKWD	4*80	BUS[00]	4*81	BUS[01]
4*82	BUS[02]	4*83	BUS[03]	4*84	BUS[04]	4*85	BUS[05]
4*86	BUS[06]	4*87	BUS[07]	4*88	BUS[08]	4*89	BUS[09]
4*90	BUS[10]	4*91	BUS[11]	4*92	BUS[12]	4*93	BUS[13]
4*94	BUS[14]	4*95	BUS[15]	4*105	-NEXT[05]	4*106	-NEXT[06]
4*107	-NEXT[07]	4*108	-NEXT[08]	4*109	-NEXT[09]	4*110	-BLOCK
4*111	-KDATA	4*112	-KSTAT	5*1	-STOP	5*6	DDR+
5*7	KSYSCLK	5*8	-AUSYSCLK	5*10	DCLK	5*20	STOPCLK
5*21	-WAKEDWT	5*22	-DVTAC	5*23	-DHTAC	5*24	-DWTAC
5*51	-F2EQ10	5*62	DBSYSCLK	5*63	DBARC	5*68	-SWAKMRT
5*69	MISYSCLK	5*70	CSYSCLK	5*71	MIARC	5*72	AUSYSCLK
5*76	-WAKEDVT	5*77	-WAKEDHT	5*80	BUS[00]	5*81	BUS[01]
5*82	BUS[02]	5*83	BUS[03]	5*84	BUS[04]	5*85	BUS[05]
5*86	BUS[06]	5*87	BUS[07]	5*88	BUS[08]	5*89	BUS[09]
5*90	BUS[10]	5*91	BUS[11]	5*92	BUS[12]	5*93	BUS[13]
5*94	BUS[14]	5*95	BUS[15]	5*109	-NEXT[09]	5*110	-BLOCK
5*114	-CURTAC	5*115	WAKECURT	5*116	-F2EQ11	6*1	OKTORUN
6*2	RESET	6*62	DBSYSCLK	6*63	DBARC	6*80	BUS[00]
6*81	BUS[01]	6*82	BUS[02]	6*83	BUS[03]	6*84	BUS[04]
6*85	BUS[05]	6*86	BUS[06]	6*87	BUS[07]	6*88	BUS[08]
6*89	BUS[09]	6*90	BUS[10]	6*91	BUS[11]	6*92	BUS[12]
6*93	BUS[13]	6*94	BUS[14]	6*95	BUS[15]	6*97	-CONST+
6*99	EMACT	6*100	ALU[00]	6*101	ALU[01]	6*102	ALU[02]
6*103	ALU[03]	6*104	ALU[04]	6*105	ALU[05]	6*106	ALU[06]
6*107	ALU[07]	6*108	ALU[08]	6*109	ALU[09]	6*110	ALU[10]
6*111	ALU[11]	6*112	ALU[12]	6*113	ALU[13]	6*114	ALU[14]
6*115	ALU[15]	7*1	-SRESET	7*2	RESET	7*6	DDR+
7*7	LOADL	7*8	-WAKEKST	7*10	-IR[00]	7*11	-IR[01]
7*12	-IR[01]	7*13	-IR[03]	7*14	-IR[04]	7*15	-IR[05]
7*16	-IR[06]	7*18	-IR[08]	7*19	-IR[09]	7*20	STOPCLK
7*21	-WAKEDWT	7*22	-DVTAC	7*23	-DHTAC	7*24	-DWTAC
7*25	-KWDTAC	7*26	SHZERO	7*28	-KSTAC	7*30	F1[0]
7*31	F1[1]	7*32	F1[2]	7*33	F1[3]	7*34	-ZEROBUS
7*36	F2[0]	7*37	F2[1]	7*38	F2[2]	7*39	F2[3]
7*40	ALUF0	7*41	ALUF1	7*42	ALUF2	7*43	ALUF3
7*44	BSZ0	7*46	-LSH1	7*47	-RSH1	7*48	-LCY8
7*49	LALUC0	7*50	SH[00]	7*51	-F2EQ10	7*54	RSEL0
7*55	RSEL1	7*56	RSEL2	7*57	RSEL3	7*59	RSEL4
7*60	-WAKE5	7*61	-PARTAC	7*62	DBSYSCLK	7*63	DBARC
7*67	-WAKEMRT	7*68	LOADR	7*69	-LOADT	7*70	-AUSYSCLK
7*71	IR+	7*72	MAR+	7*73	-STORE	7*74	SEL37
7*75	DNS	7*76	-WAKEDVT	7*77	-WAKEDHT	7*78	-IR[07]
7*79	-WAKEKWD	7*80	BUS[00]	7*81	BUS[01]	7*82	BUS[02]
7*83	BUS[03]	7*84	BUS[04]	7*85	BUS[05]	7*86	BUS[06]
7*87	BUS[07]	7*88	BUS[08]	7*89	BUS[09]	7*90	BUS[10]

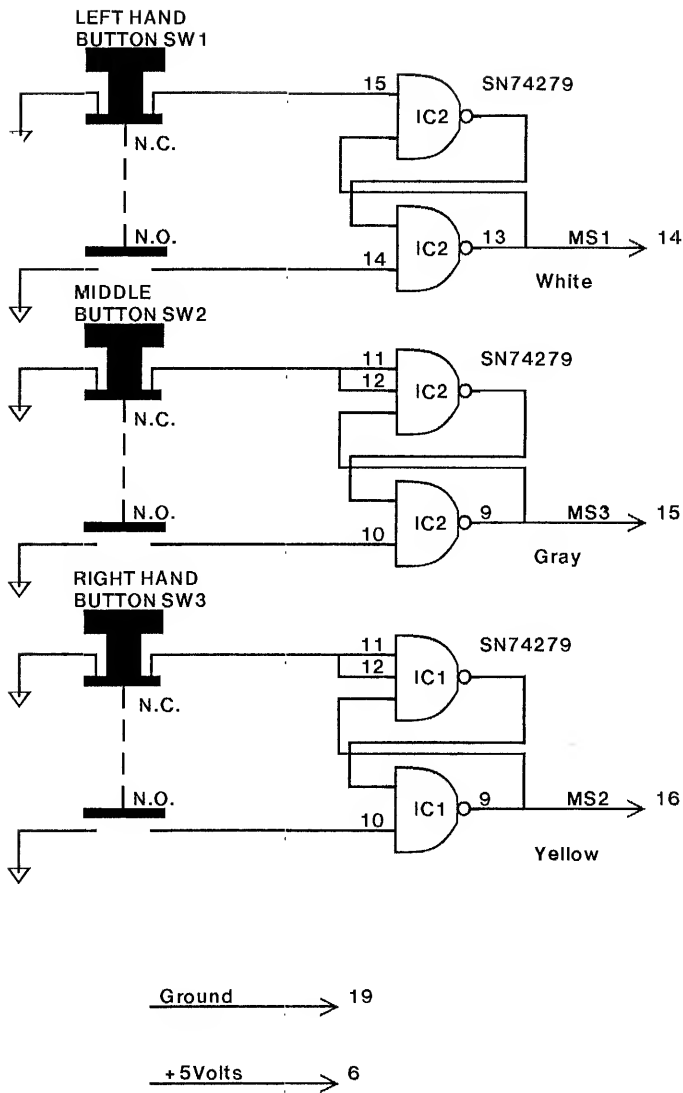
7*91	BUS[11]	7*92	BUS[12]	7*93	BUS[13]	7*94	BUS[14]
7*95	BUS[15]	7*96	-<MD	7*97	-CONST<	7*98	<DISP
7*99	EMACT	7*100	-ETAC	7*101	-6ACT	7*102	-5ACT
7*103	-WAKEET	7*104	-WAKE6	7*105	-NEXT[05]	7*106	-NEXT[06]
7*107	-NEXT[07]	7*108	-NEXT[08]	7*109	-NEXT[09]	7*110	-BLOCK
7*111	-<KDATA	7*112	-<KSTAT	7*114	-CURTAC	7*115	WAKECURT
7*116	-F2EQ11	7*117	-READMOUS	7*118	-WAKEPART	7*120	BS0
7*121	BS1	7*122	BS2	8*7	LOADL	8*8	-AUSYSCLK
8*10	-IR[00]	8*11	-IR[01]	8*12	-IR[01]	8*13	-IR[03]
8*14	-IR[04]	8*15	-IR[05]	8*16	-IR[06]	8*18	-IR[08]
8*19	-IR[09]	8*20	-IR[10]	8*21	-IR[11]	8*22	-IR[12]
8*23	-IR[12]	8*24	-IR[14]	8*25	-IR[15]	8*26	SHZERO
8*34	-ZEROBUS	8*36	F2[0]	8*37	F2[1]	8*38	F2[2]
8*40	ALUF0	8*41	ALUF1	8*42	ALUF2	8*43	ALUF3
8*44	BSZ0	8*46	-LSH1	8*47	-RSH1	8*48	-LCY8
8*49	LALUC0	8*50	SH[00]	8*54	RSEL0	8*55	RSEL1
8*56	RSEL2	8*57	RSEL3	8*59	RSEL4	8*68	LOADR
8*69	-LOADT	8*71	IR<	8*72	AUSYSCLK	8*73	CARRY
8*74	SKIP	8*75	DNS	8*78	-IR[07]	8*80	BUS[00]
8*81	BUS[01]	8*82	BUS[02]	8*83	BUS[03]	8*84	BUS[04]
8*85	BUS[05]	8*86	BUS[06]	8*87	BUS[07]	8*88	BUS[08]
8*89	BUS[09]	8*90	BUS[10]	8*91	BUS[11]	8*92	BUS[12]
8*93	BUS[13]	8*94	BUS[14]	8*95	BUS[15]	8*98	<DISP
8*99	EMACT	8*100	ALU[00]	8*101	ALU[01]	8*102	ALU[02]
8*103	ALU[03]	8*104	ALU[04]	8*105	ALU[05]	8*106	ALU[06]
8*107	ALU[07]	8*108	ALU[08]	8*109	ALU[09]	8*110	ALU[10]
8*111	ALU[11]	8*112	ALU[12]	8*113	ALU[13]	8*114	ALU[14]
8*115	ALU[15]	8*116	-F2EQ11	9*1	-STOP	9*2	RESET
9*6	RS7	9*7	RS6	9*8	RS4	9*10	RS2
9*11	RS5	9*12	RS1	9*13	-PC	9*14	-CE
9*15	-CS0	9*16	RS0	9*18	-DS1	9*19	-DS0
9*20	-MD[00]	9*21	-MD[01]	9*22	-MD[02]	9*23	-MD[03]
9*24	-MD[04]	9*25	-MD[05]	9*26	-MD[06]	9*28	-MD[07]
9*29	-MD[08]	9*30	-MD[09]	9*31	-MD[10]	9*32	-MD[11]
9*33	-MD[12]	9*34	-MD[13]	9*36	-MD[14]	9*37	-MD[15]
9*38	READPAR	9*39	MAR[06]	9*40	MAR[05]	9*41	MAR[07]
9*42	MAR[08]	9*43	MAR[14]	9*44	MAR[11]	9*46	MAR[13]
9*47	XMAR[15]	9*48	XIOREF	9*49	WRITEPAR	9*50	MAR[09]
9*51	MAR[12]	9*52	MAR[10]	9*54	RSEL0	9*55	RSEL1
9*56	RSEL2	9*57	RSEL3	9*59	RSEL4	9*61	-PARTAC
9*62	-SRESET	9*67	-WAKEMRT	9*68	-SWAKMRT	9*69	MISYSCLK
9*70	RS3	9*71	MIARC	9*72	MAR<	9*73	-STORE
9*74	SELR37	9*75	-CS1	9*76	-CS2	9*77	-CS3
9*78	-W1	9*79	-W0	9*80	BUS[00]	9*81	BUS[01]
9*82	BUS[02]	9*83	BUS[03]	9*84	BUS[04]	9*85	BUS[05]
9*86	BUS[06]	9*87	BUS[07]	9*88	BUS[08]	9*89	BUS[09]
9*90	BUS[10]	9*91	BUS[11]	9*92	BUS[12]	9*93	BUS[13]
9*94	BUS[14]	9*95	BUS[15]	9*96	-<MD	9*97	-CONST<
9*98	XMT2	9*100	ALU[00]	9*101	ALU[01]	9*102	ALU[02]
9*103	ALU[03]	9*104	ALU[04]	9*105	ALU[05]	9*106	ALU[06]
9*107	ALU[07]	9*108	ALU[08]	9*109	ALU[09]	9*110	ALU[10]
9*111	ALU[11]	9*112	ALU[12]	9*113	ALU[13]	9*114	ALU[14]
9*115	ALU[15]	9*117	-READMOUS	9*118	-WAKEPART	9*120	BS0
9*121	BS1	9*122	BS2	10*20	-MD[00]	10*21	-MD[01]
10*22	-MD[02]	10*23	-MD[03]	10*24	-MD[04]	10*25	-MD[05]
10*26	-MD[06]	10*28	-MD[07]	10*29	-MD[08]	10*30	-MD[09]
10*31	-MD[10]	10*32	-MD[11]	10*33	-MD[12]	10*34	-MD[13]
10*36	-MD[14]	10*37	-MD[15]	10*41	MAR[07]	10*42	MAR[08]
10*43	MAR[14]	10*44	MAR[11]	10*46	MAR[13]	10*47	XMAR[15]
10*48	XIOREF	10*50	MAR[09]	10*51	MAR[12]	10*52	MAR[10]
10*69	MISYSCLK	10*71	MIARC	10*98	XMT2	11*20	-MD[00]
11*21	-MD[01]	11*22	-MD[02]	11*23	-MD[03]	11*24	-MD[04]
11*25	-MD[05]	11*26	-MD[06]	11*28	-MD[07]	11*29	-MD[08]
11*30	-MD[09]	11*31	-MD[10]	11*32	-MD[11]	11*33	-MD[12]
11*34	-MD[13]	11*36	-MD[14]	11*37	-MD[15]	11*41	MAR[07]
11*42	MAR[08]	11*43	MAR[14]	11*44	MAR[11]	11*46	MAR[13]
11*47	XMAR[15]	11*48	XIOREF	11*50	MAR[09]	11*51	MAR[12]
11*52	MAR[10]	11*69	MISYSCLK	11*71	MIARC	11*98	XMT2
12*20	-MD[00]	12*21	-MD[01]	12*22	-MD[02]	12*23	-MD[03]
12*24	-MD[04]	12*25	-MD[05]	12*26	-MD[06]	12*28	-MD[07]
12*29	-MD[08]	12*30	-MD[09]	12*31	-MD[10]	12*32	-MD[11]
12*33	-MD[12]	12*34	-MD[13]	12*36	-MD[14]	12*37	-MD[15]
12*41	MAR[07]	12*42	MAR[08]	12*43	MAR[14]	12*44	MAR[11]
12*46	MAR[13]	12*47	XMAR[15]	12*48	XIOREF	12*50	MAR[09]
12*51	MAR[12]	12*52	MAR[10]	12*69	MISYSCLK	12*71	MIARC
12*98	XMT2	13*67	RS7	13*68	RS6	13*69	RS4
13*70	RS3	13*71	RS2	13*72	RS5	13*73	RS1
13*74	-PC	13*75	-CE	13*76	-CS0	13*77	RS0
13*78	-W0	13*79	-DS0	13*80	-MD[02]	13*81	-MD[00]

13*82 -MD[01]	13*83 -MD[03]	13*84 -MD[01]	13*85 -MD[00]
13*86 -MD[02]	13*87 -MD[03]	13*88 -MD[04]	13*89 -MD[05]
13*90 -MD[04]	13*91 -MD[05]	13*92 -MD[07]	13*93 -MD[06]
13*94 -MD[06]	13*95 -MD[07]	13*96 -MD[08]	13*97 -MD[09]
13*98 -MD[10]	13*99 -MD[11]	13*100 MAR[06]	13*101 MAR[05]
13*102 MAR[07]	13*103 MAR[08]	13*104 MAR[14]	13*105 MAR[11]
13*106 MAR[13]	13*107 -MD[08]	13*108 -MD[09]	13*109 -MD[10]
13*110 -MD[11]	13*111 MAR[09]	13*112 MAR[12]	13*113 MAR[10]
14*67 RS7	14*68 RS6	14*69 RS4	14*70 RS3
14*71 RS2	14*72 RS5	14*73 RS1	14*74 -PC
14*75 -CE	14*76 -CS0	14*77 RS0	14*78 -W0
14*79 -DS0	14*92 -MD[12]	14*95 -MD[12]	14*96 -MD[13]
14*97 -MD[14]	14*98 -MD[15]	14*99 READPAR	14*100 MAR[06]
14*101 MAR[05]	14*102 MAR[07]	14*103 MAR[08]	14*104 MAR[14]
14*105 MAR[11]	14*106 MAR[13]	14*107 -MD[13]	14*108 -MD[14]
14*109 -MD[15]	14*110 WRITEPAR	14*111 MAR[09]	14*112 MAR[12]
14*113 MAR[10]	15*67 RS7	15*68 RS6	15*69 RS4
15*70 RS3	15*71 RS2	15*72 RS5	15*73 RS1
15*74 -PC	15*75 -CE	15*76 -CS0	15*77 RS0
15*78 -W1	15*79 -DS1	15*80 -MD[02]	15*81 -MD[00]
15*82 -MD[01]	15*83 -MD[03]	15*84 -MD[01]	15*85 -MD[00]
15*86 -MD[02]	15*87 -MD[03]	15*88 -MD[04]	15*89 -MD[05]
15*90 -MD[04]	15*91 -MD[05]	15*92 -MD[07]	15*93 -MD[06]
15*94 -MD[06]	15*95 -MD[07]	15*96 -MD[08]	15*97 -MD[09]
15*98 -MD[10]	15*99 -MD[11]	15*100 MAR[06]	15*101 MAR[05]
15*102 MAR[07]	15*103 MAR[08]	15*104 MAR[14]	15*105 MAR[11]
15*106 MAR[13]	15*107 -MD[08]	15*108 -MD[09]	15*109 -MD[10]
15*110 -MD[11]	15*111 MAR[09]	15*112 MAR[12]	15*113 MAR[10]
16*67 RS7	16*68 RS6	16*69 RS4	16*70 RS3
16*71 RS2	16*72 RS5	16*73 RS1	16*74 -PC
16*75 -CE	16*76 -CS0	16*77 RS0	16*78 -W1
16*79 -DS1	16*92 -MD[12]	16*95 -MD[12]	16*96 -MD[13]
16*97 -MD[14]	16*98 -MD[15]	16*99 READPAR	16*100 MAR[06]
16*101 MAR[05]	16*102 MAR[07]	16*103 MAR[08]	16*104 MAR[14]
16*105 MAR[11]	16*106 MAR[13]	16*107 -MD[13]	16*108 -MD[14]
16*109 -MD[15]	16*110 WRITEPAR	16*111 MAR[09]	16*112 MAR[12]
16*113 MAR[10]	17*67 RS7	17*68 RS6	17*69 RS4
17*70 RS3	17*71 RS2	17*72 RS5	17*73 RS1
17*74 -PC	17*75 -CE	17*76 -CS1	17*77 RS0
17*78 -W0	17*79 -DS0	17*80 -MD[02]	17*81 -MD[00]
17*82 -MD[01]	17*83 -MD[03]	17*84 -MD[01]	17*85 -MD[00]
17*86 -MD[02]	17*87 -MD[03]	17*88 -MD[04]	17*89 -MD[05]
17*90 -MD[04]	17*91 -MD[05]	17*92 -MD[07]	17*93 -MD[06]
17*94 -MD[06]	17*95 -MD[07]	17*96 -MD[08]	17*97 -MD[09]
17*98 -MD[10]	17*99 -MD[11]	17*100 MAR[06]	17*101 MAR[05]
17*102 MAR[07]	17*103 MAR[08]	17*104 MAR[14]	17*105 MAR[11]
17*106 MAR[13]	17*107 -MD[08]	17*108 -MD[09]	17*109 -MD[10]
17*110 -MD[11]	17*111 MAR[09]	17*112 MAR[12]	17*113 MAR[10]
18*67 RS7	18*68 RS6	18*69 RS4	18*70 RS3
18*71 RS2	18*72 RS5	18*73 RS1	18*74 -PC
18*75 -CE	18*76 -CS1	18*77 RS0	18*78 -W0
18*79 -DS0	18*92 -MD[12]	18*95 -MD[12]	18*96 -MD[13]
18*97 -MD[14]	18*98 -MD[15]	18*99 READPAR	18*100 MAR[06]
18*101 MAR[05]	18*102 MAR[07]	18*103 MAR[08]	18*104 MAR[14]
18*105 MAR[11]	18*106 MAR[13]	18*107 -MD[13]	18*108 -MD[14]
18*109 -MD[15]	18*110 WRITEPAR	18*111 MAR[09]	18*112 MAR[12]
18*113 MAR[10]	19*67 RS7	19*68 RS6	19*69 RS4
19*70 RS3	19*71 RS2	19*72 RS5	19*73 RS1
19*74 -PC	19*75 -CE	19*76 -CS1	19*77 RS0
19*78 -W1	19*79 -DS1	19*80 -MD[02]	19*81 -MD[00]
19*82 -MD[01]	19*83 -MD[03]	19*84 -MD[01]	19*85 -MD[00]
19*86 -MD[02]	19*87 -MD[03]	19*88 -MD[04]	19*89 -MD[05]
19*90 -MD[04]	19*91 -MD[05]	19*92 -MD[07]	19*93 -MD[06]
19*94 -MD[06]	19*95 -MD[07]	19*96 -MD[08]	19*97 -MD[09]
19*98 -MD[10]	19*99 -MD[11]	19*100 MAR[06]	19*101 MAR[05]
19*102 MAR[07]	19*103 MAR[08]	19*104 MAR[14]	19*105 MAR[11]
19*106 MAR[13]	19*107 -MD[08]	19*108 -MD[09]	19*109 -MD[10]
19*110 -MD[11]	19*111 MAR[09]	19*112 MAR[12]	19*113 MAR[10]
20*67 RS7	20*68 RS6	20*69 RS4	20*70 RS3
20*71 RS2	20*72 RS5	20*73 RS1	20*74 -PC
20*75 -CE	20*76 -CS1	20*77 RS0	20*78 -W1
20*79 -DS1	20*92 -MD[12]	20*95 -MD[12]	20*96 -MD[13]
20*97 -MD[14]	20*98 -MD[15]	20*99 READPAR	20*100 MAR[06]
20*101 MAR[05]	20*102 MAR[07]	20*103 MAR[08]	20*104 MAR[14]
20*105 MAR[11]	20*106 MAR[13]	20*107 -MD[13]	20*108 -MD[14]
20*109 -MD[15]	20*110 WRITEPAR	20*111 MAR[09]	20*112 MAR[12]
20*113 MAR[10]	21*67 RS7	21*68 RS6	21*69 RS4
21*70 RS3	21*71 RS2	21*72 RS5	21*73 RS1
21*74 -PC	21*75 -CE	21*76 -CS2	21*77 RS0

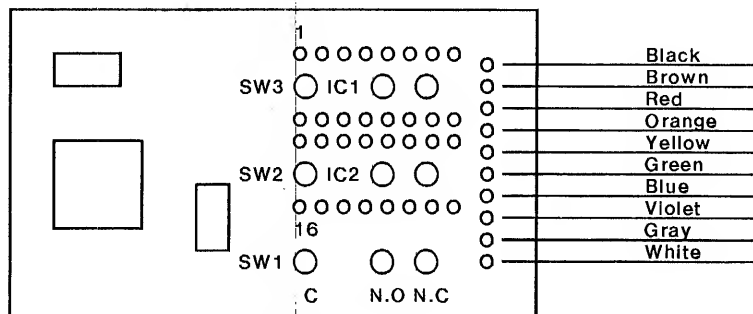
21*78 -W0	21*79 -DS0	21*80 -MD[02]	21*81 -MD[00]
21*82 -MD[01]	21*83 -MD[03]	21*84 -MD[01]	21*85 -MD[00]
21*86 -MD[02]	21*87 -MD[03]	21*88 -MD[04]	21*89 -MD[05]
21*90 -MD[04]	21*91 -MD[05]	21*92 -MD[07]	21*93 -MD[06]
21*94 -MD[06]	21*95 -MD[07]	21*96 -MD[08]	21*97 -MD[09]
21*98 -MD[10]	21*99 -MD[11]	21*100 MAR[06]	21*101 MAR[05]
21*102 MAR[07]	21*103 MAR[08]	21*104 MAR[14]	21*105 MAR[11]
21*106 MAR[13]	21*107 -MD[08]	21*108 -MD[09]	21*109 -MD[10]
21*110 -MD[11]	21*111 MAR[09]	21*112 MAR[12]	21*113 MAR[10]
22*67 RS7	22*68 RS6	22*69 RS4	22*70 RS3
22*71 RS2	22*72 RS5	22*73 RS1	22*74 -PC
22*75 -CE	22*76 -CS2	22*77 RS0	22*78 -W0
22*79 -DS0	22*92 -MD[12]	22*95 -MD[12]	22*96 -MD[13]
22*97 -MD[14]	22*98 -MD[15]	22*99 READPAR	22*100 MAR[06]
22*101 MAR[05]	22*102 MAR[07]	22*103 MAR[08]	22*104 MAR[14]
22*105 MAR[11]	22*106 MAR[13]	22*107 -MD[13]	22*108 -MD[14]
22*109 -MD[15]	22*110 WRITEPAR	22*111 MAR[09]	22*112 MAR[12]
22*113 MAR[10]	23*67 RS7	23*68 RS6	23*69 RS4
23*70 RS3	23*71 RS2	23*72 RS5	23*73 RS1
23*74 -PC	23*75 -CE	23*76 -CS2	23*77 RS0
23*78 -W1	23*79 -DS1	23*80 -MD[02]	23*81 -MD[00]
23*82 -MD[01]	23*83 -MD[03]	23*84 -MD[01]	23*85 -MD[00]
23*86 -MD[02]	23*87 -MD[03]	23*88 -MD[04]	23*89 -MD[05]
23*90 -MD[04]	23*91 -MD[05]	23*92 -MD[07]	23*93 -MD[06]
23*94 -MD[06]	23*95 -MD[07]	23*96 -MD[08]	23*97 -MD[09]
23*98 -MD[10]	23*99 -MD[11]	23*100 MAR[06]	23*101 MAR[05]
23*102 MAR[07]	23*103 MAR[08]	23*104 MAR[14]	23*105 MAR[11]
23*106 MAR[13]	23*107 -MD[08]	23*108 -MD[09]	23*109 -MD[10]
23*110 -MD[11]	23*111 MAR[09]	23*112 MAR[12]	23*113 MAR[10]
24*67 RS7	24*68 RS6	24*69 RS4	24*70 RS3
24*71 RS2	24*72 RS5	24*73 RS1	24*74 -PC
24*75 -CE	24*76 -CS2	24*77 RS0	24*78 -W1
24*79 -DS1	24*92 -MD[12]	24*95 -MD[12]	24*96 -MD[13]
24*97 -MD[14]	24*98 -MD[15]	24*99 READPAR	24*100 MAR[06]
24*101 MAR[05]	24*102 MAR[07]	24*103 MAR[08]	24*104 MAR[14]
24*105 MAR[11]	24*106 MAR[13]	24*107 -MD[13]	24*108 -MD[14]
24*109 -MD[15]	24*110 WRITEPAR	24*111 MAR[09]	24*112 MAR[12]
24*113 MAR[10]	25*67 RS7	25*68 RS6	25*69 RS4
25*70 RS3	25*71 RS2	25*72 RS5	25*73 RS1
25*74 -PC	25*75 -CE	25*76 -CS3	25*77 RS0
25*78 -W0	25*79 -DS0	25*80 -MD[02]	25*81 -MD[00]
25*82 -MD[01]	25*83 -MD[03]	25*84 -MD[01]	25*85 -MD[00]
25*86 -MD[02]	25*87 -MD[03]	25*88 -MD[04]	25*89 -MD[05]
25*90 -MD[04]	25*91 -MD[05]	25*92 -MD[07]	25*93 -MD[06]
25*94 -MD[06]	25*95 -MD[07]	25*96 -MD[08]	25*97 -MD[09]
25*98 -MD[10]	25*99 -MD[11]	25*100 MAR[06]	25*101 MAR[05]
25*102 MAR[07]	25*103 MAR[08]	25*104 MAR[14]	25*105 MAR[11]
25*106 MAR[13]	25*107 -MD[08]	25*108 -MD[09]	25*109 -MD[10]
25*110 -MD[11]	25*111 MAR[09]	25*112 MAR[12]	25*113 MAR[10]
26*67 RS7	26*68 RS6	26*69 RS4	26*70 RS3
26*71 RS2	26*72 RS5	26*73 RS1	26*74 -PC
26*75 -CE	26*76 -CS3	26*77 RS0	26*78 -W0
26*79 -DS0	26*92 -MD[12]	26*95 -MD[12]	26*96 -MD[13]
26*97 -MD[14]	26*98 -MD[15]	26*99 READPAR	26*100 MAR[06]
26*101 MAR[05]	26*102 MAR[07]	26*103 MAR[08]	26*104 MAR[14]
26*105 MAR[11]	26*106 MAR[13]	26*107 -MD[13]	26*108 -MD[14]
26*109 -MD[15]	26*110 WRITEPAR	26*111 MAR[09]	26*112 MAR[12]
26*113 MAR[10]	27*67 RS7	27*68 RS6	27*69 RS4
27*70 RS3	27*71 RS2	27*72 RS5	27*73 RS1
27*74 -PC	27*75 -CE	27*76 -CS3	27*77 RS0
27*78 -W1	27*79 -DS1	27*80 -MD[02]	27*81 -MD[00]
27*82 -MD[01]	27*83 -MD[03]	27*84 -MD[01]	27*85 -MD[00]
27*86 -MD[02]	27*87 -MD[03]	27*88 -MD[04]	27*89 -MD[05]
27*90 -MD[04]	27*91 -MD[05]	27*92 -MD[07]	27*93 -MD[06]
27*94 -MD[06]	27*95 -MD[07]	27*96 -MD[08]	27*97 -MD[09]
27*98 -MD[10]	27*99 -MD[11]	27*100 MAR[06]	27*101 MAR[05]
27*102 MAR[07]	27*103 MAR[08]	27*104 MAR[14]	27*105 MAR[11]
27*106 MAR[13]	27*107 -MD[08]	27*108 -MD[09]	27*109 -MD[10]
27*110 -MD[11]	27*111 MAR[09]	27*112 MAR[12]	27*113 MAR[10]
28*67 RS7	28*68 RS6	28*69 RS4	28*70 RS3
28*71 RS2	28*72 RS5	28*73 RS1	28*74 -PC
28*75 -CE	28*76 -CS3	28*77 RS0	28*78 -W1
28*79 -DS1	28*92 -MD[12]	28*95 -MD[12]	28*96 -MD[13]
28*97 -MD[14]	28*98 -MD[15]	28*99 READPAR	28*100 MAR[06]
28*101 MAR[05]	28*102 MAR[07]	28*103 MAR[08]	28*104 MAR[14]
28*105 MAR[11]	28*106 MAR[13]	28*107 -MD[13]	28*108 -MD[14]
28*109 -MD[15]	28*110 WRITEPAR	28*111 MAR[09]	28*112 MAR[12]
28*113 MAR[10] +L			

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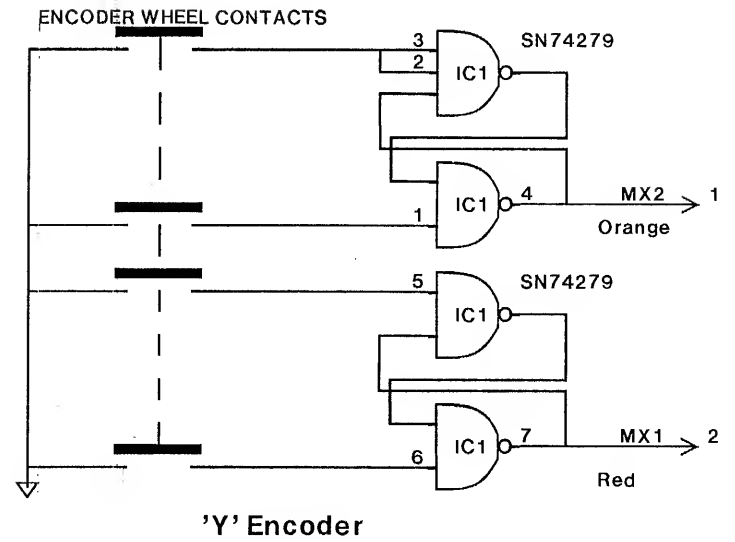
# Alto Mouse Circuitry



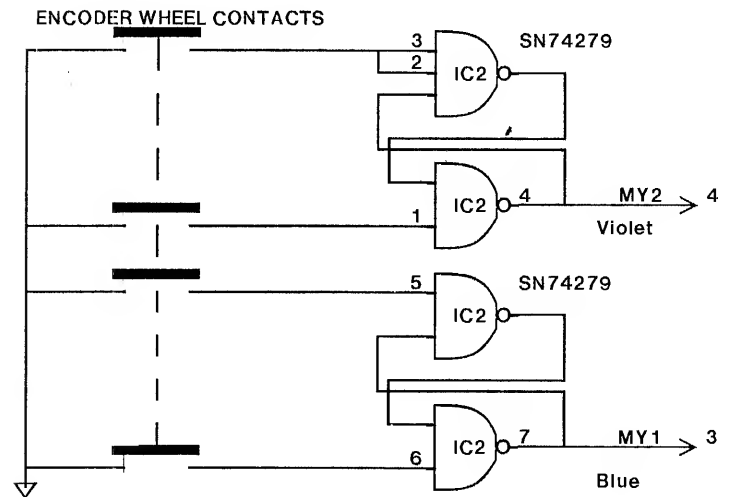
THESE REPRESENT  
MOUSE CONNECTOR  
PIN NUMBERS



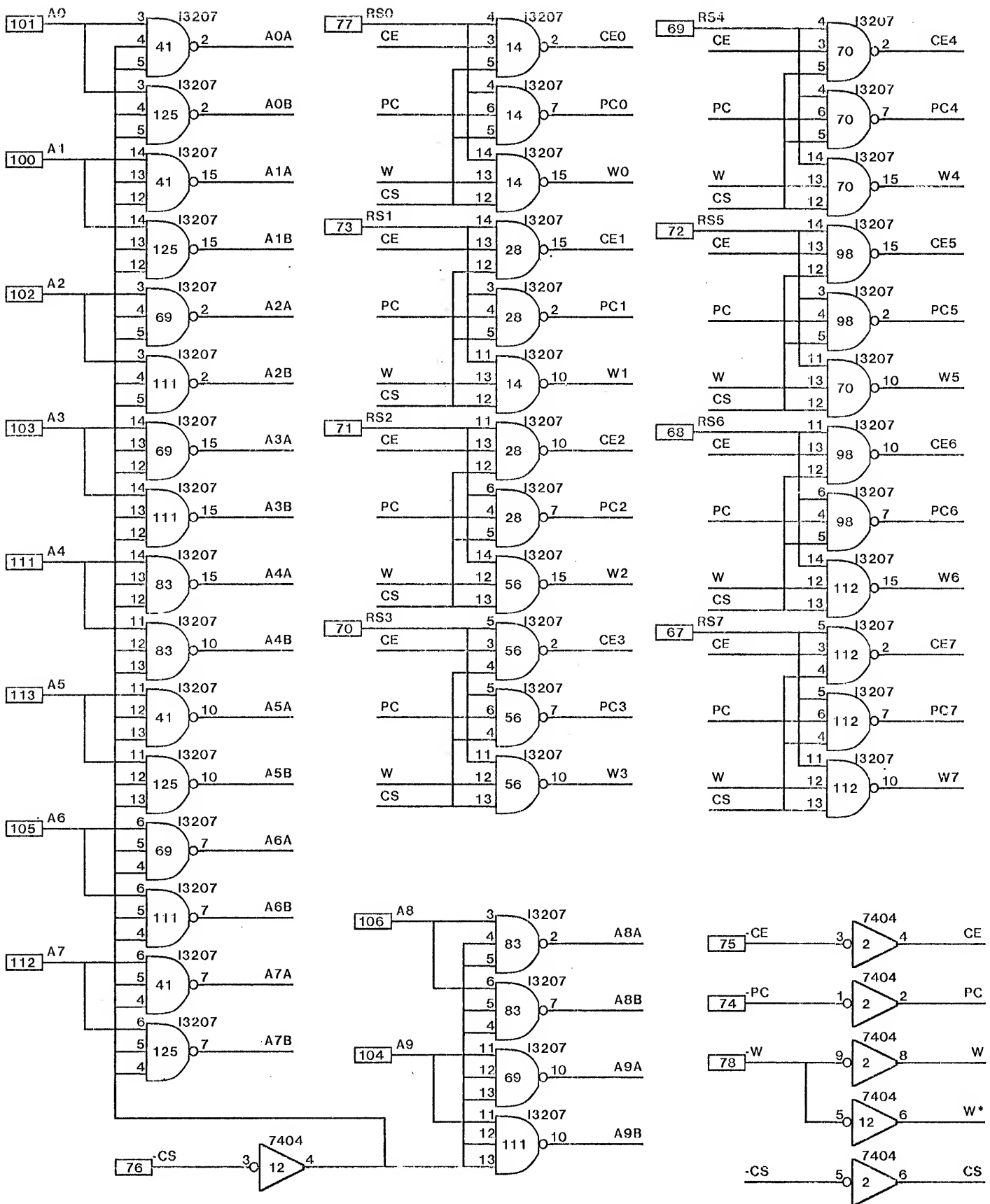
Mouse P.C.B.

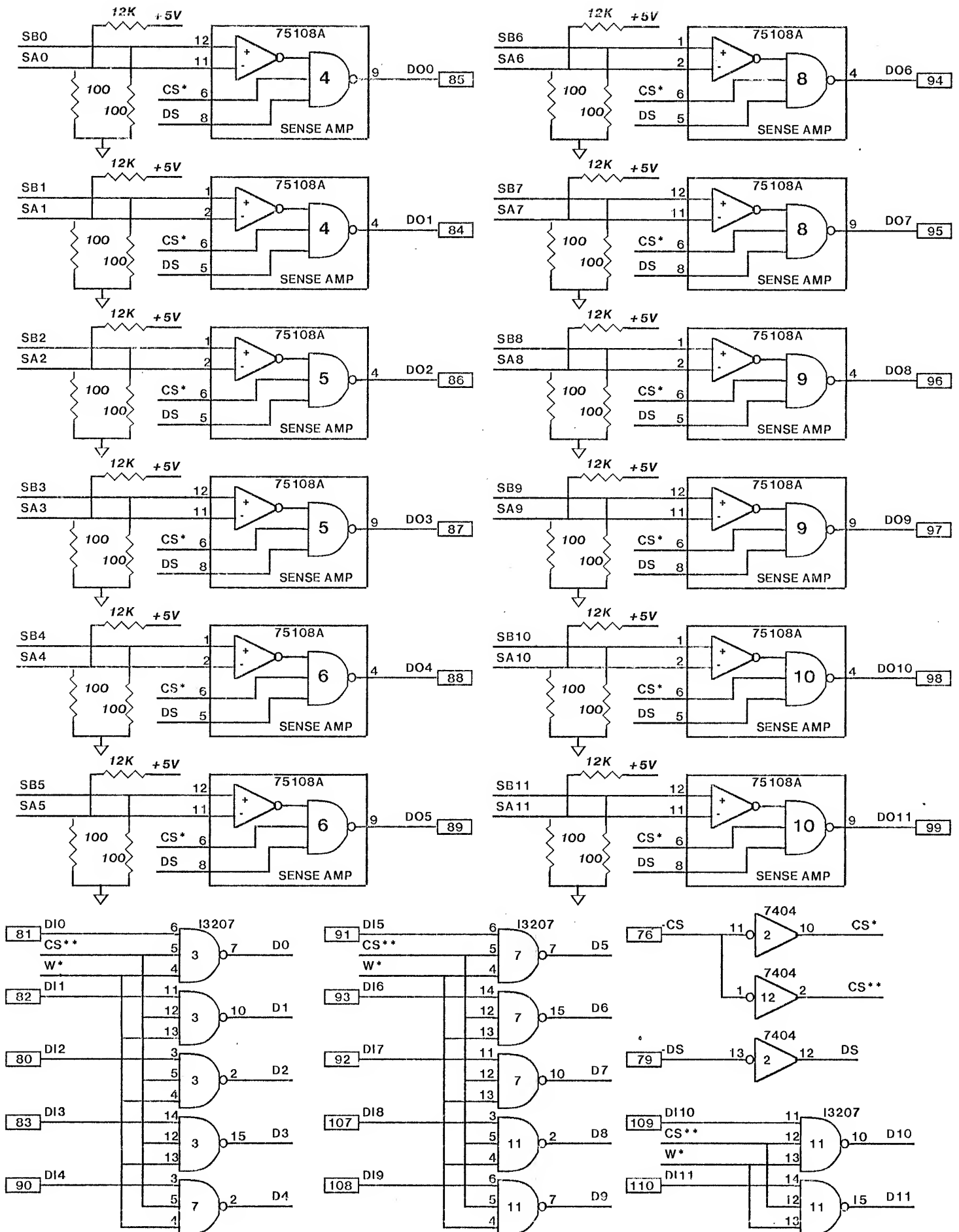


'Y' Encoder



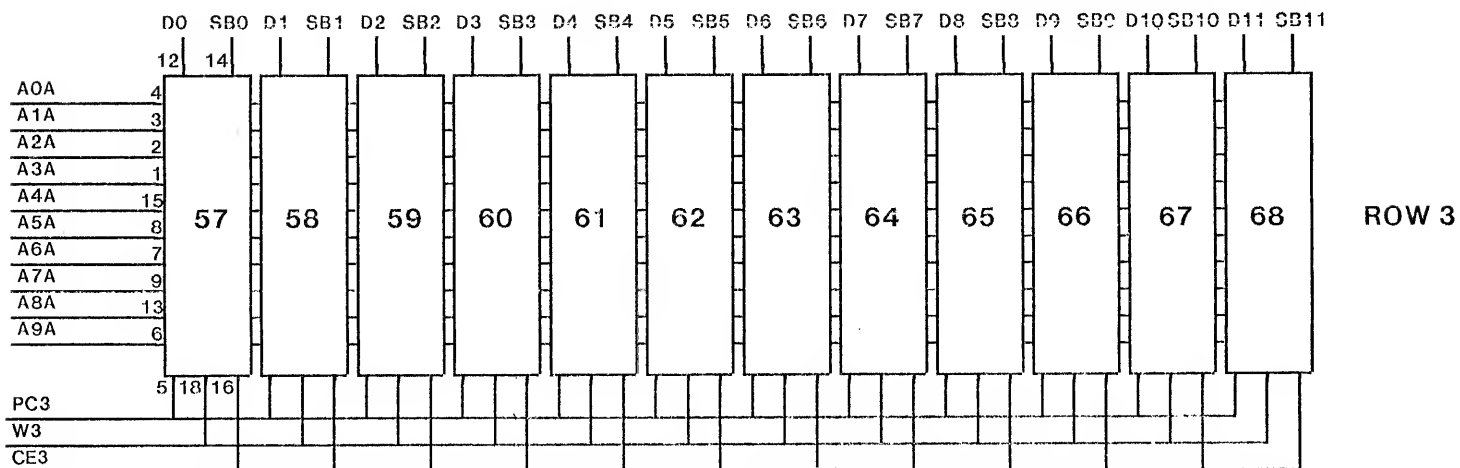
'X' Encoder



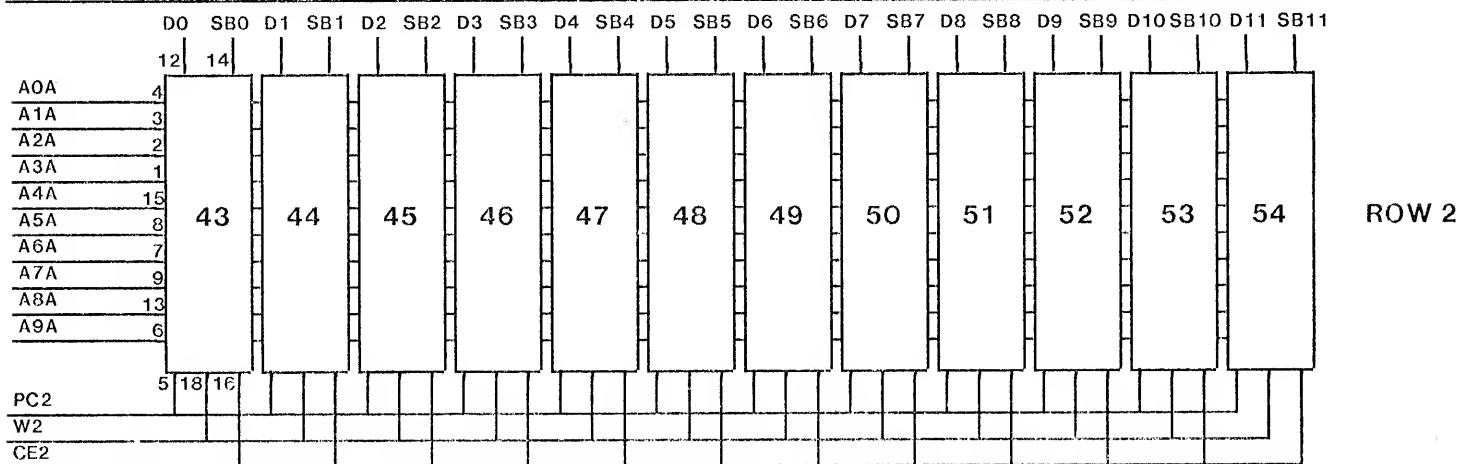


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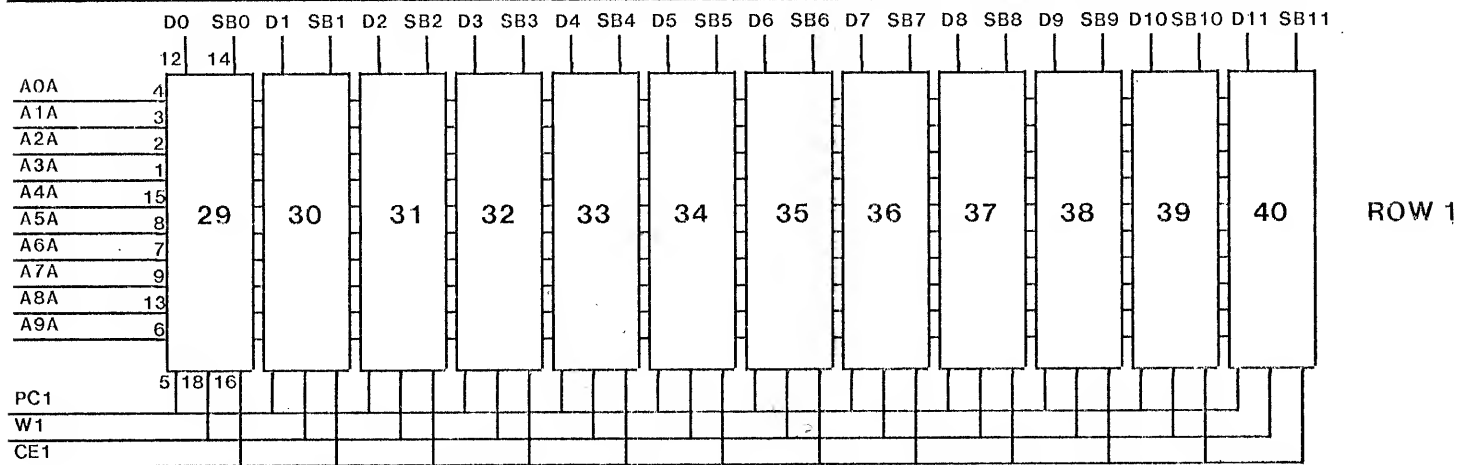
ALTO MOS MEMORY Page 3



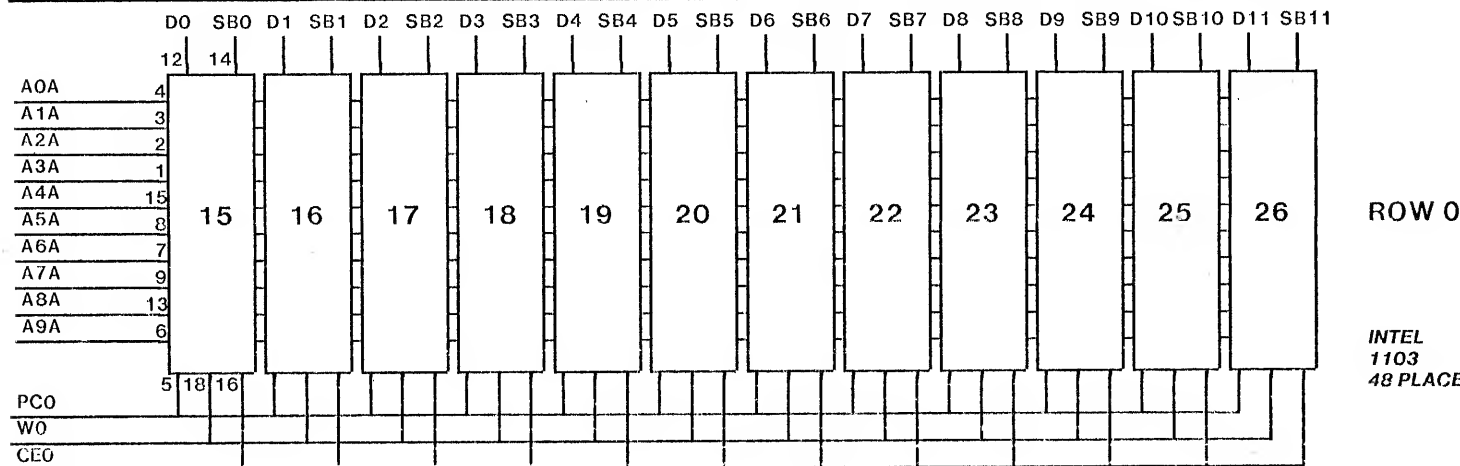
ROW 3



ROW 2



ROW 1

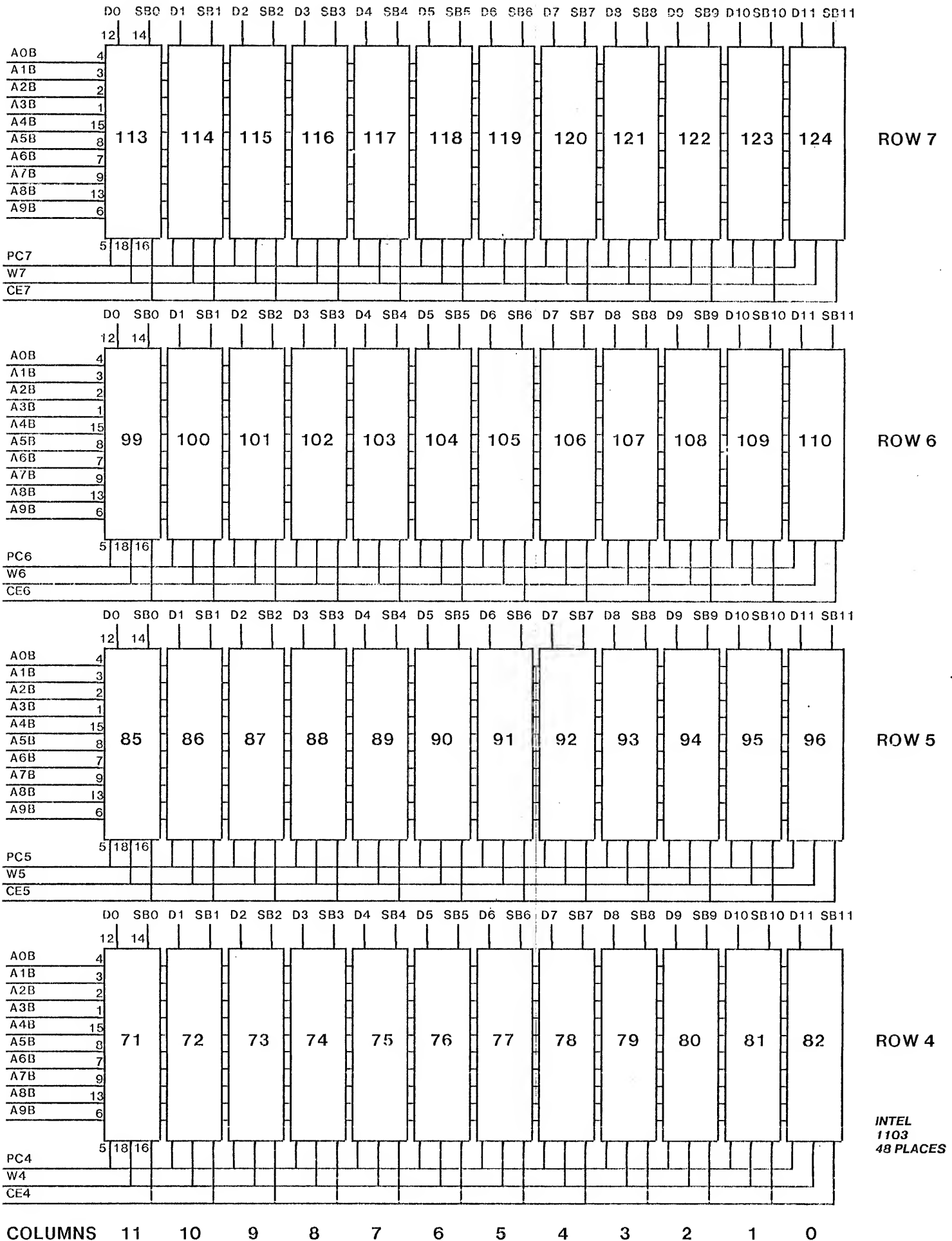


ROW 0

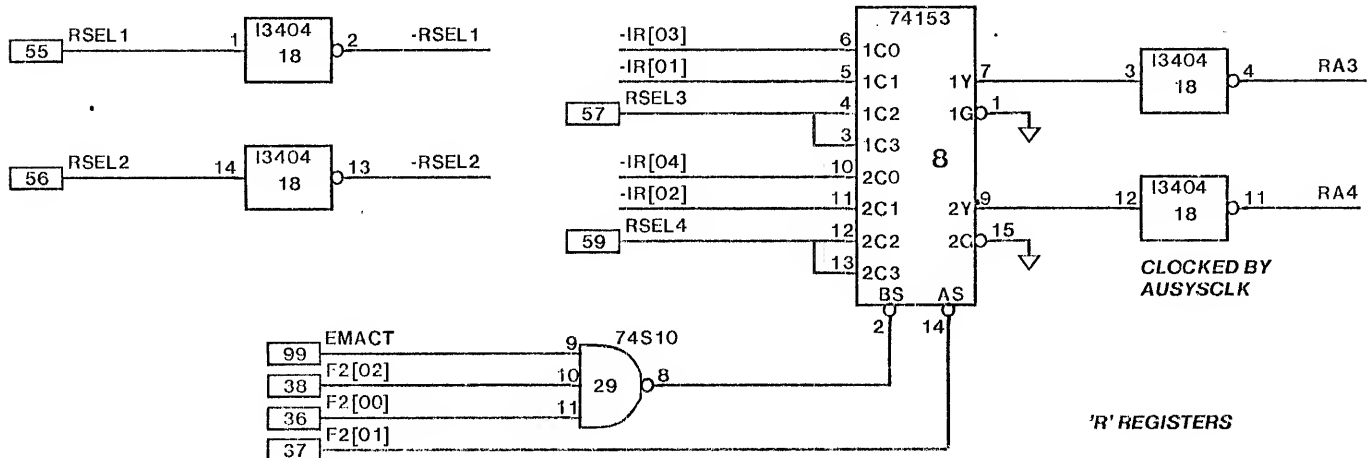
INTEL  
1103  
48 PLACES

COLUMNS 11 10 9 8 7 6 5 4 3 2 1 0



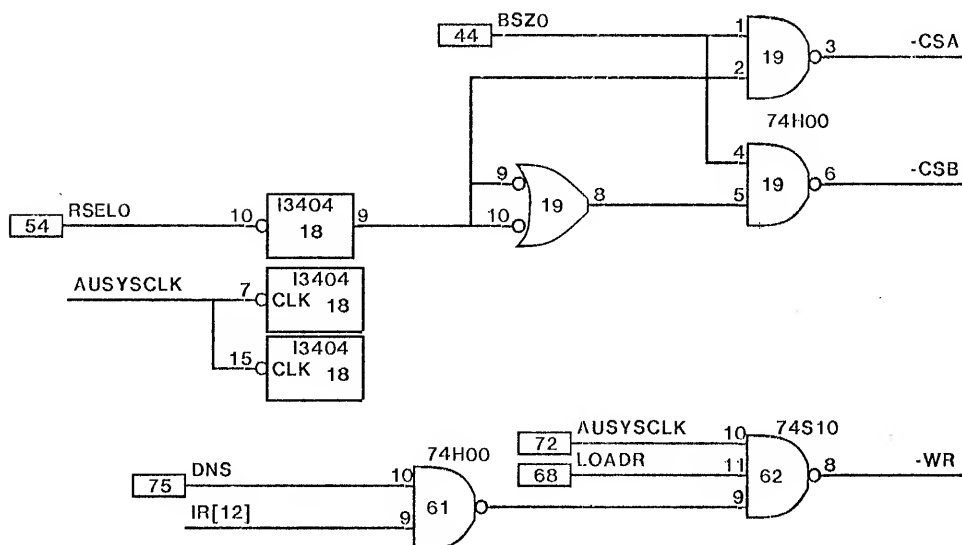


ALU Page 1

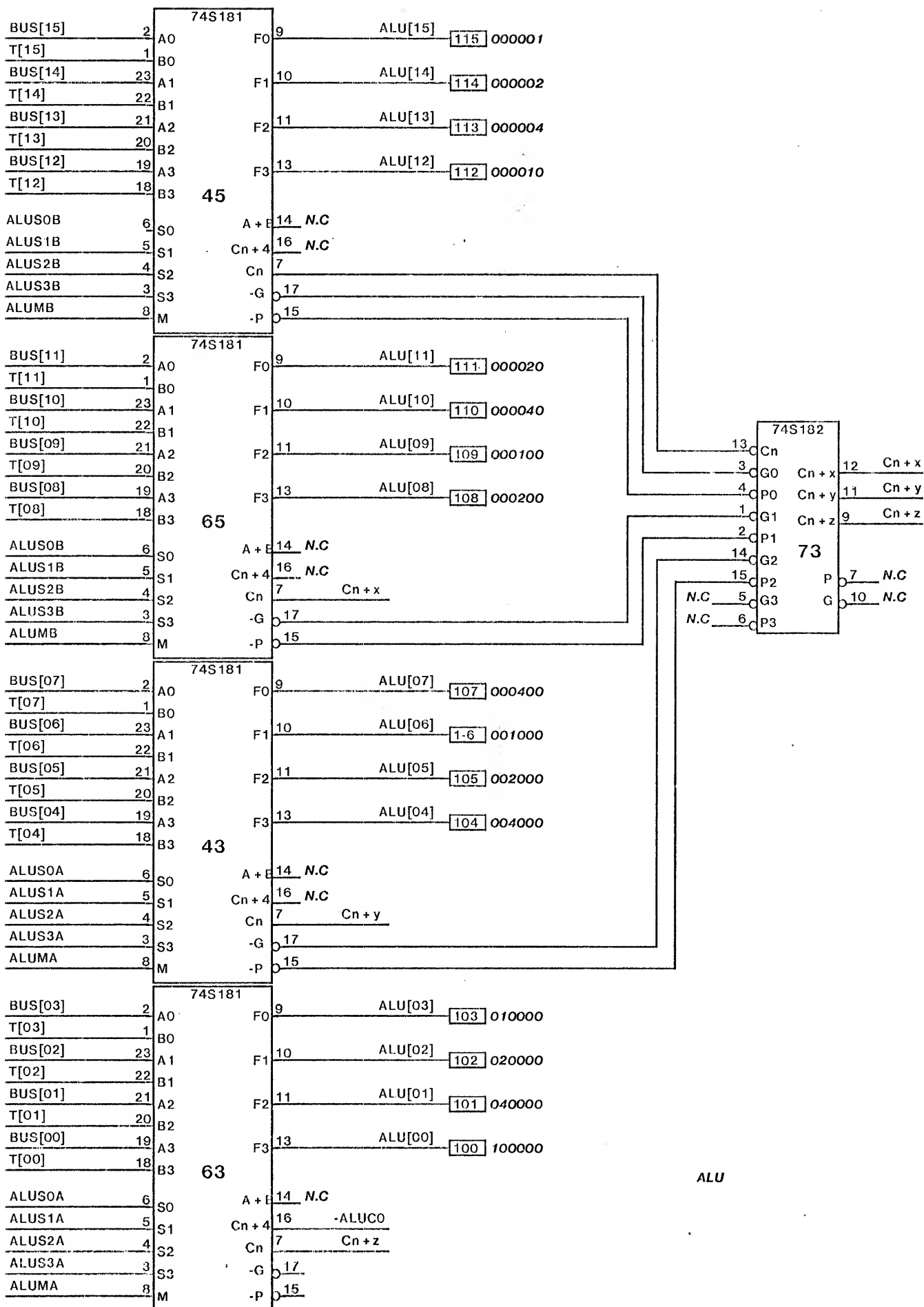


## 'R' REGISTERS

ALU Page 2

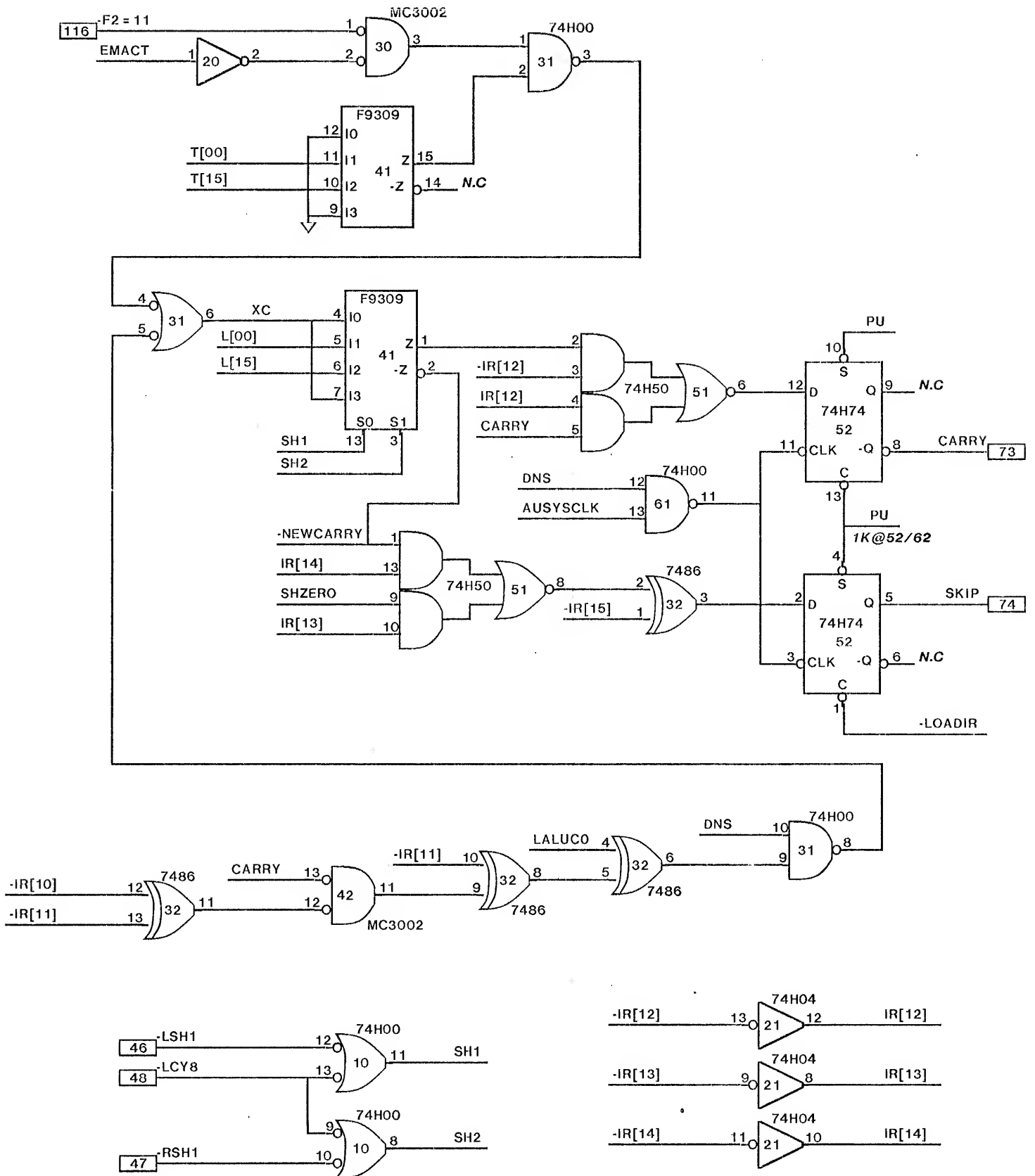


### ALU CONTROL



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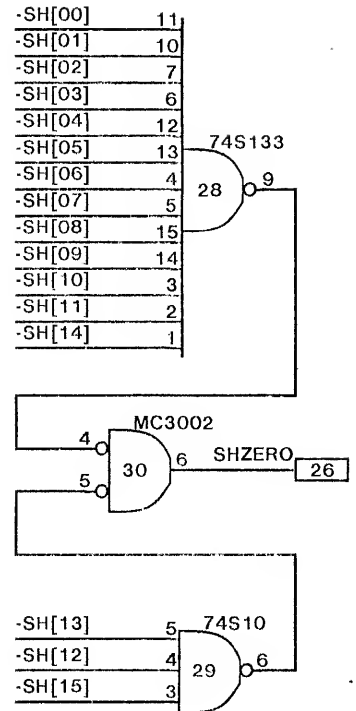
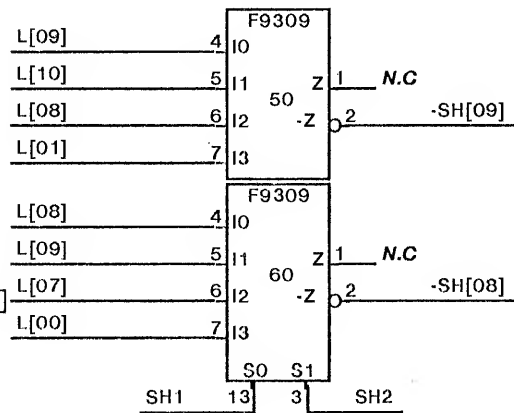
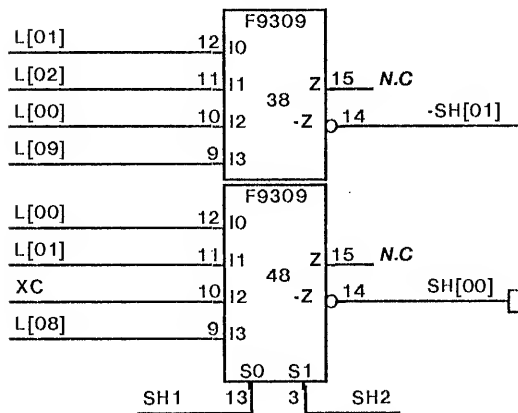
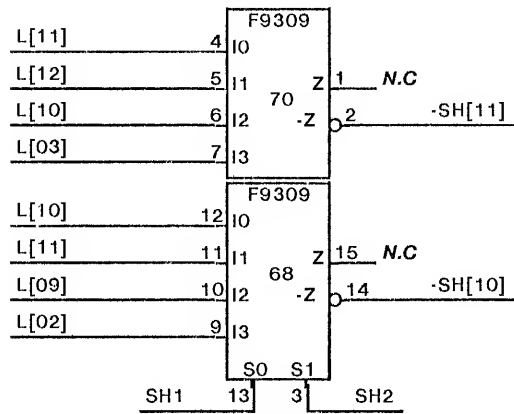
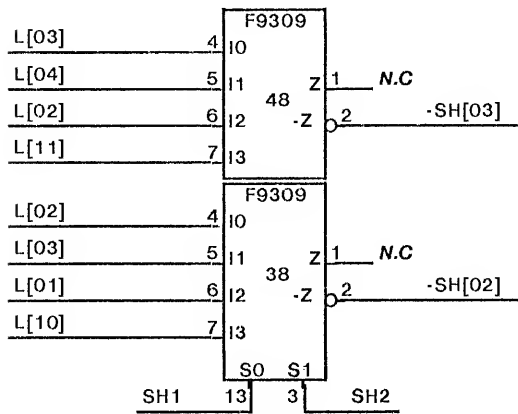
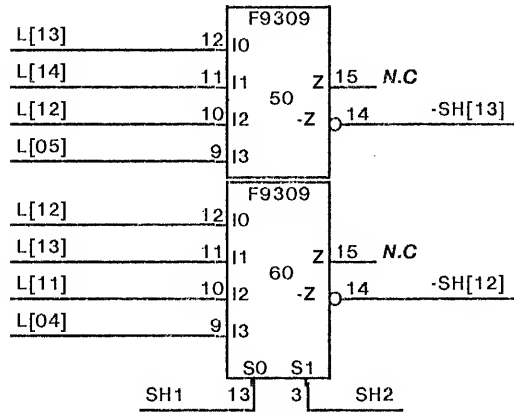
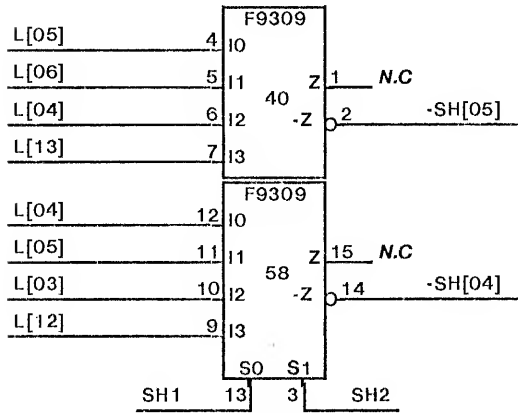
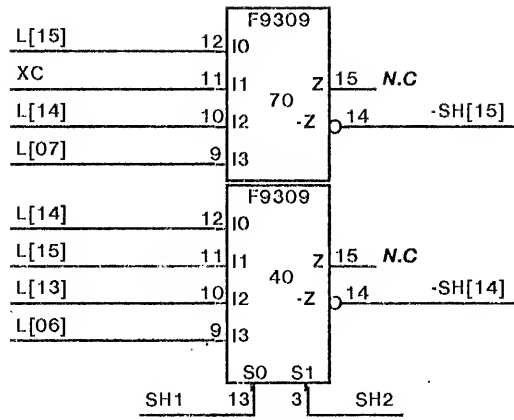
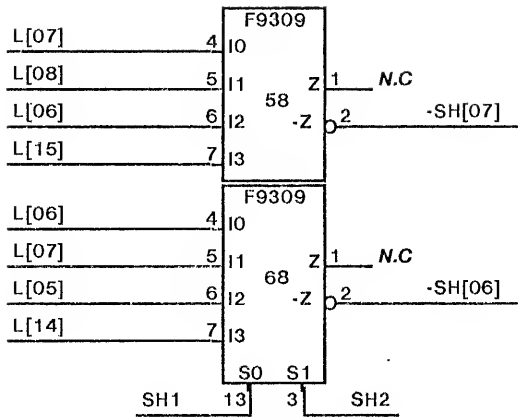
ALU Page 4



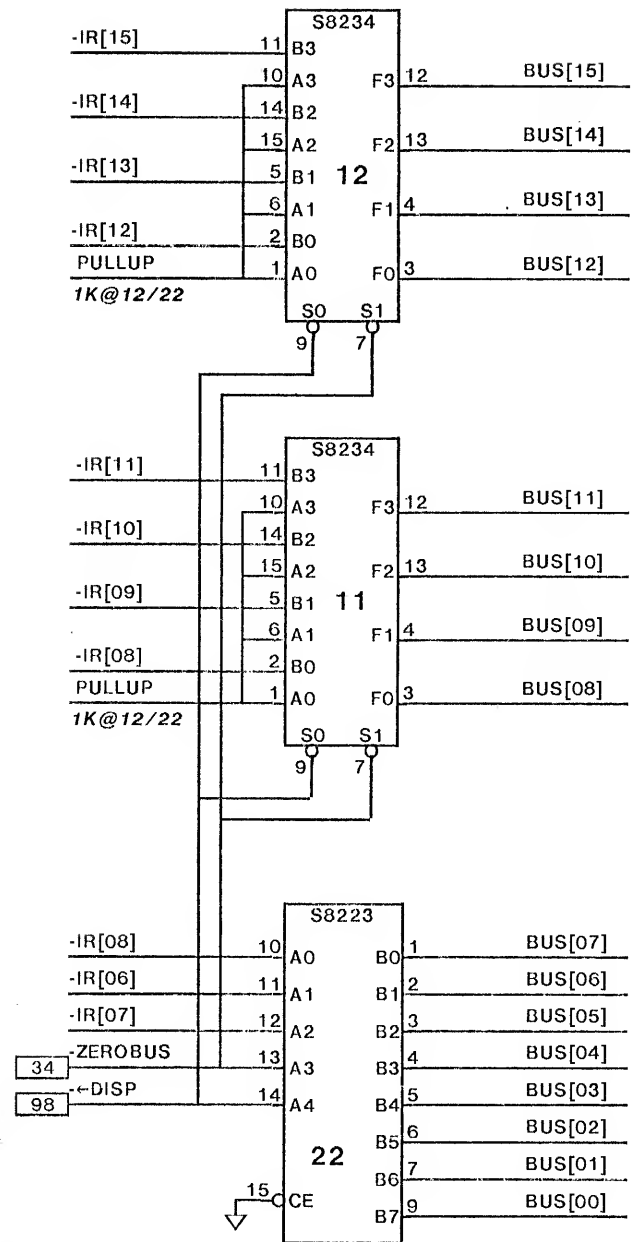
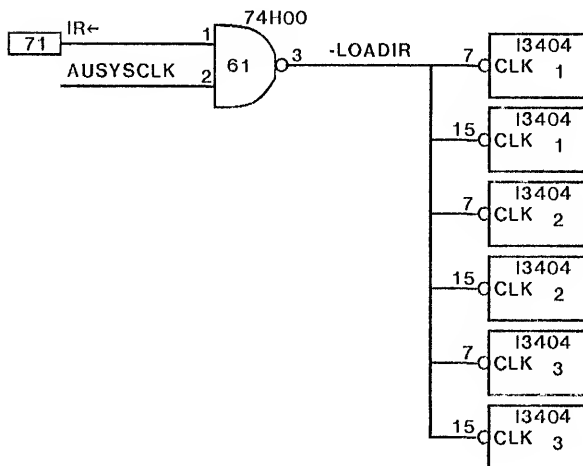
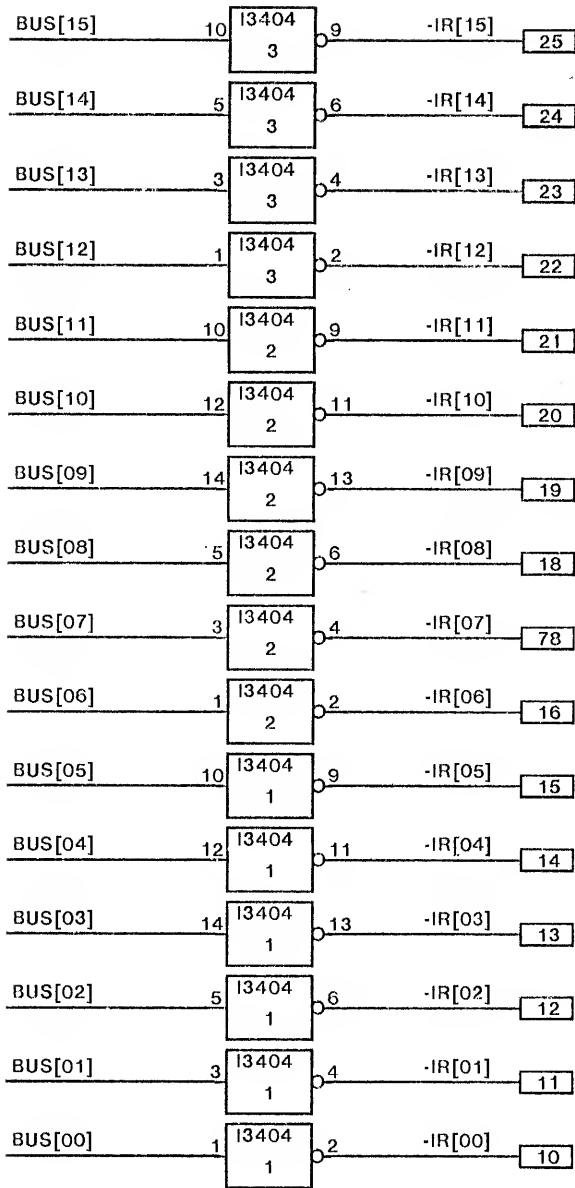
SKIP/CARRY

ALU Page 5





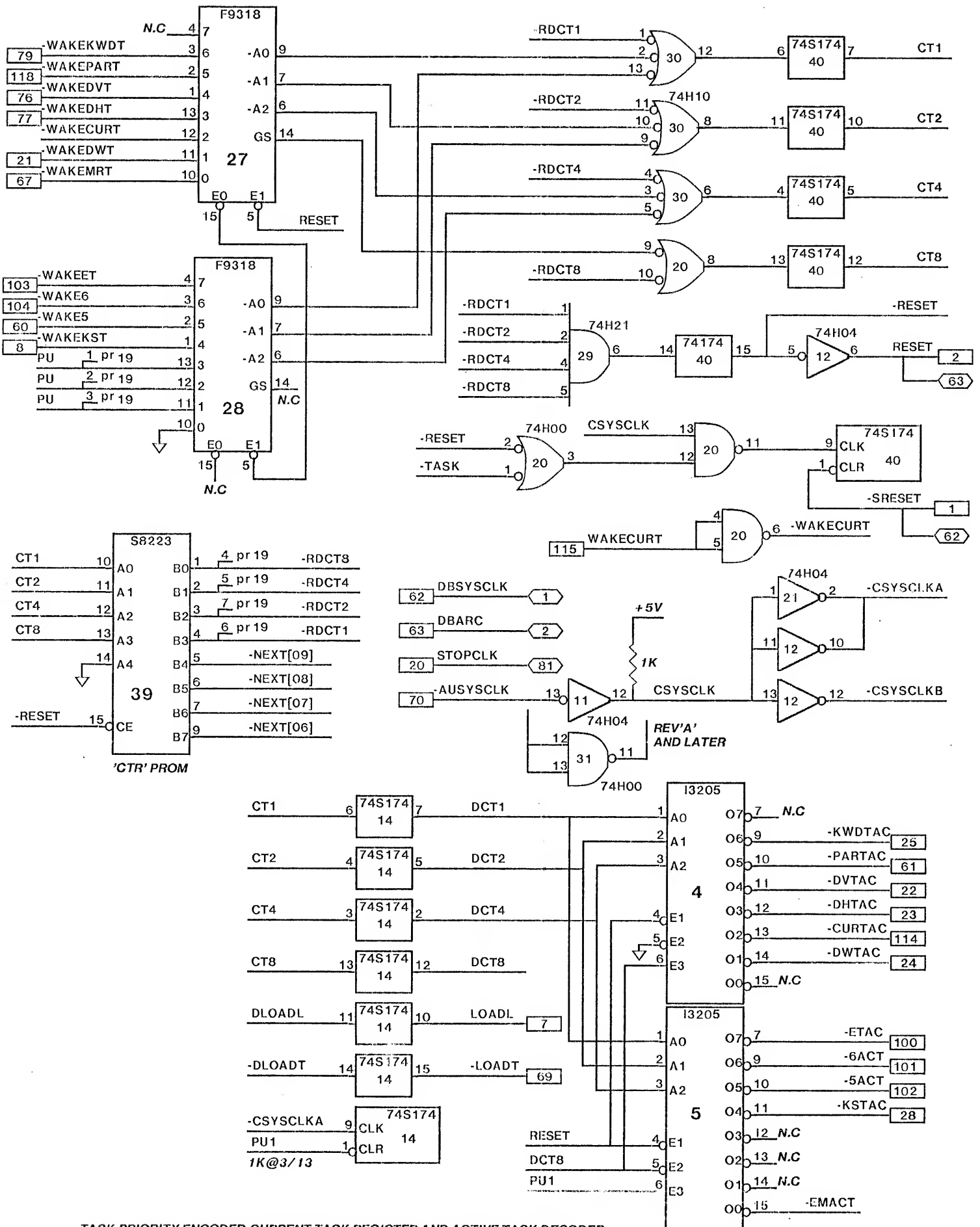
ARITHMETIC SHIFTER



'DISPLAY' PROM

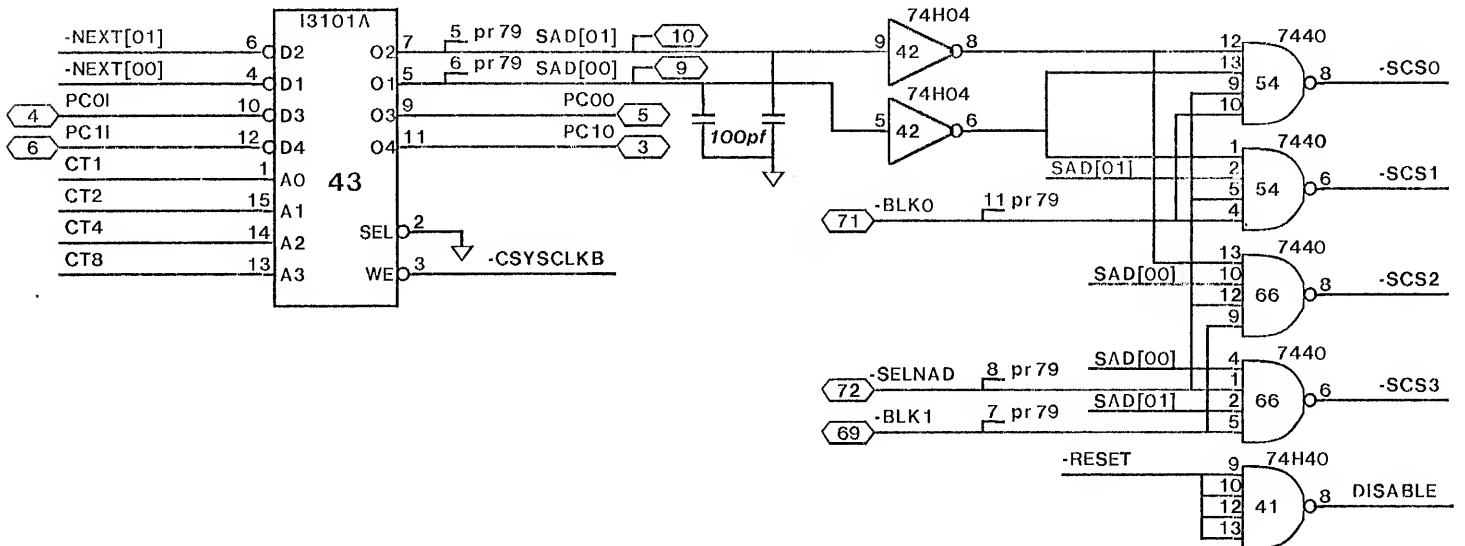
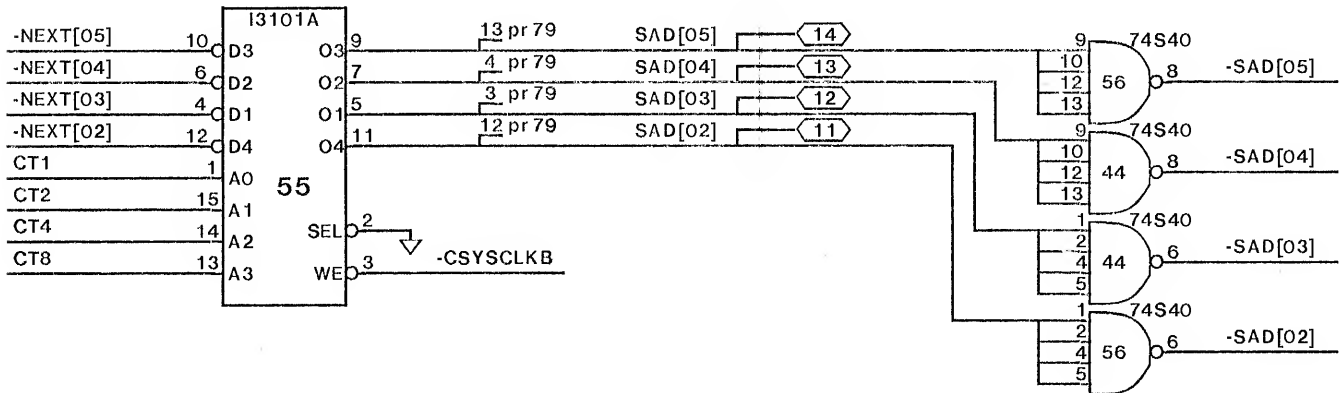
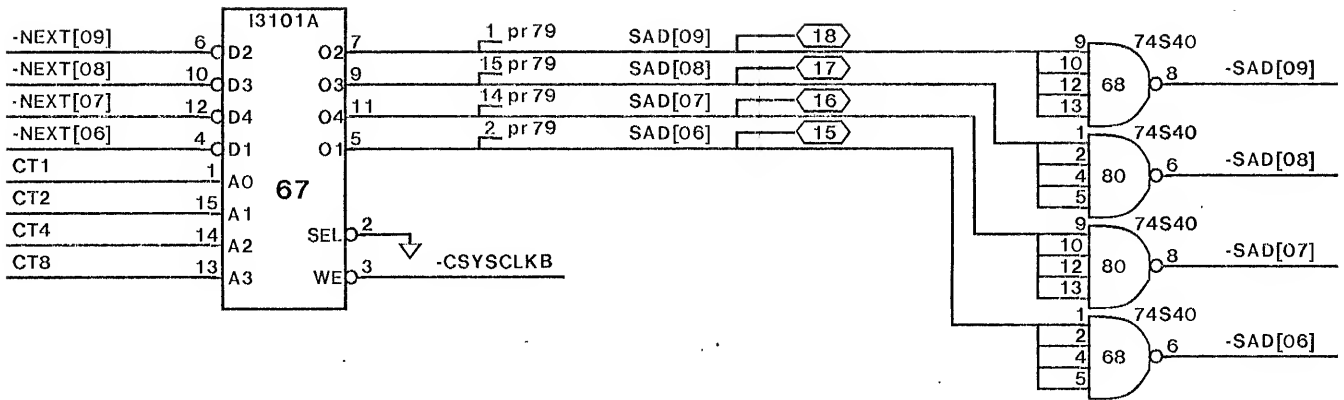
INSTRUCTION REGISTER



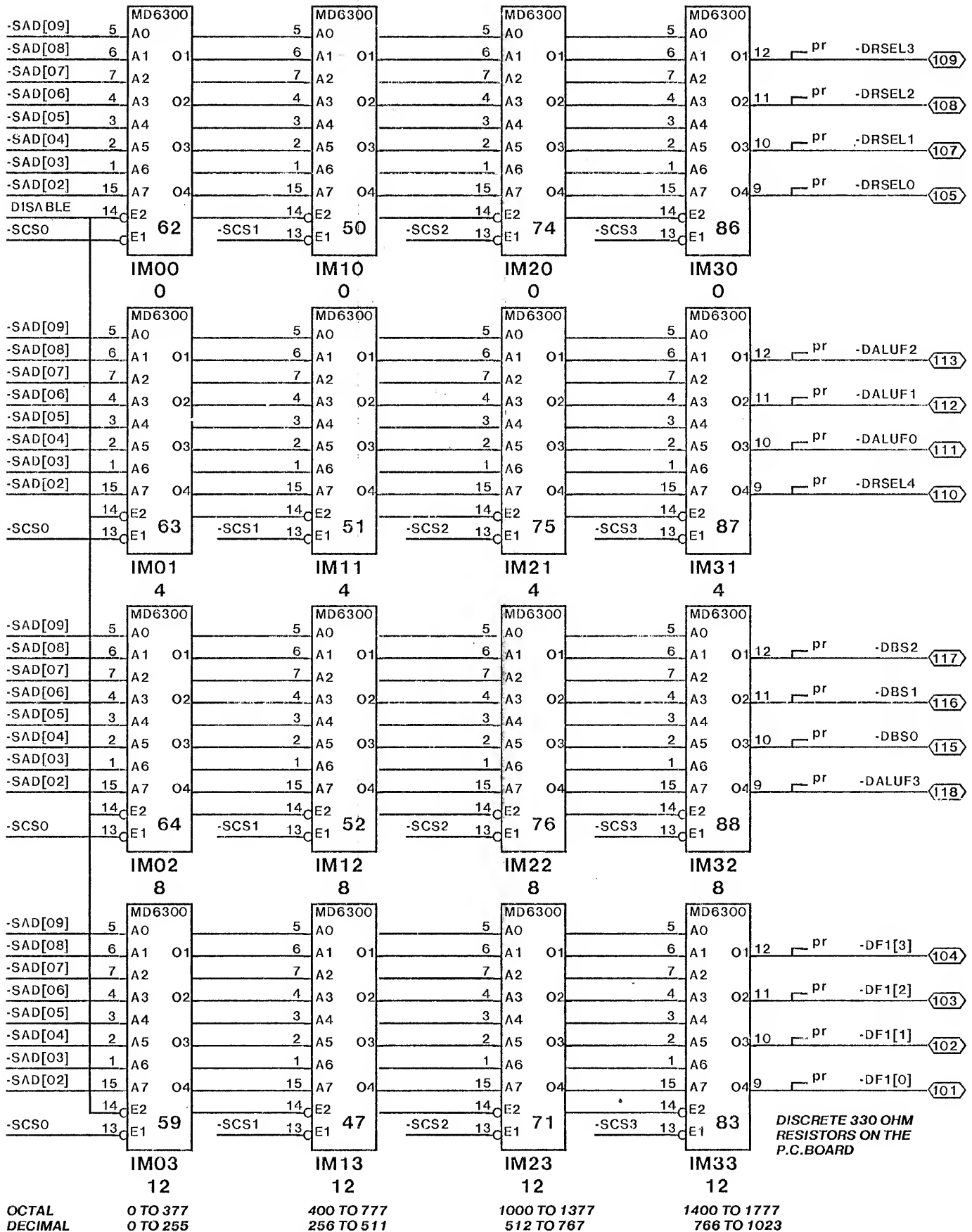


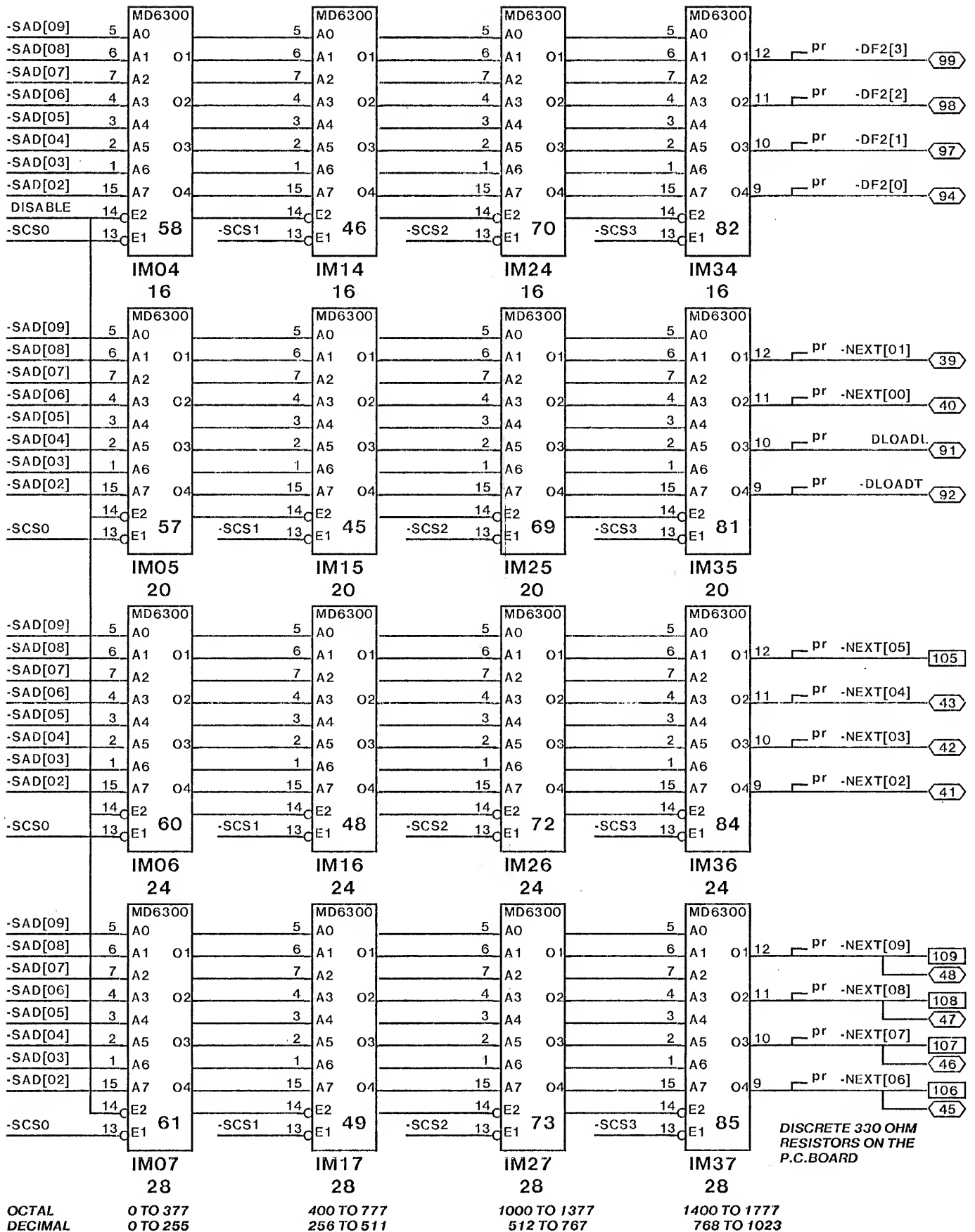
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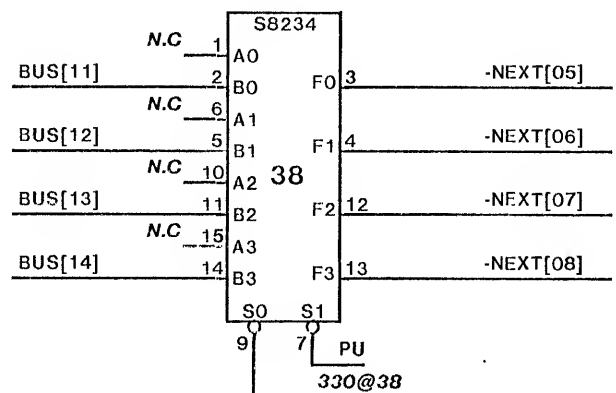
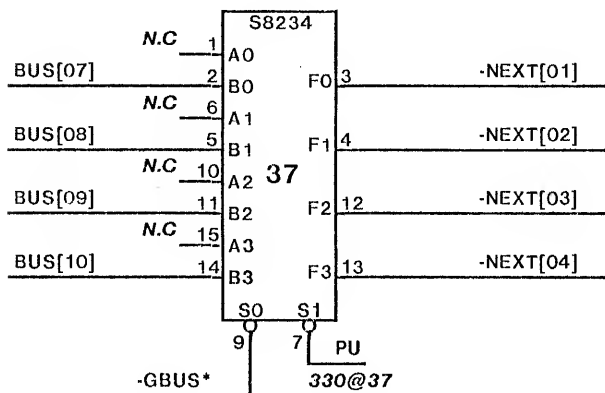
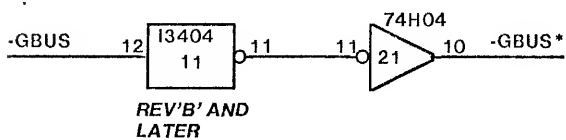
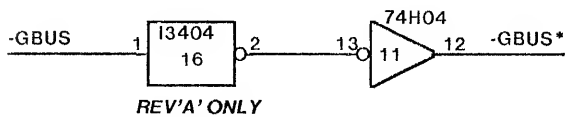
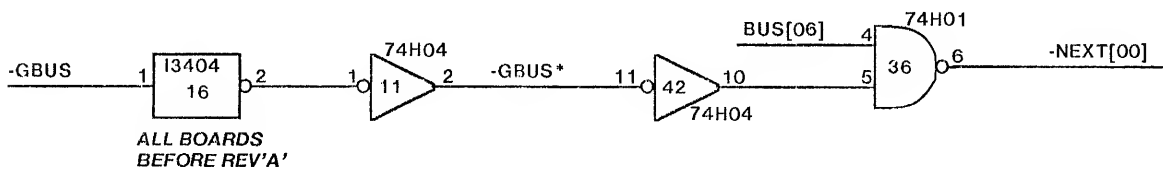
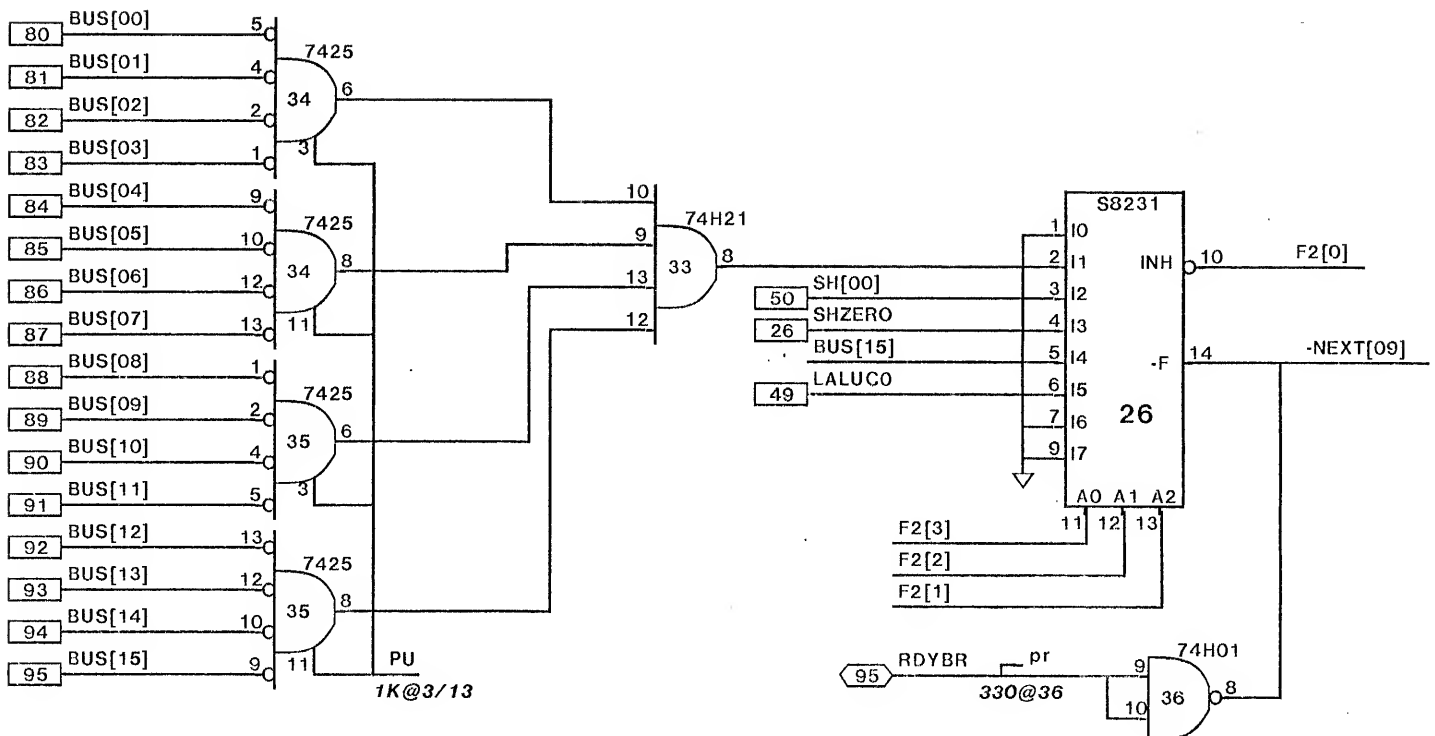
CONTROL Page 2



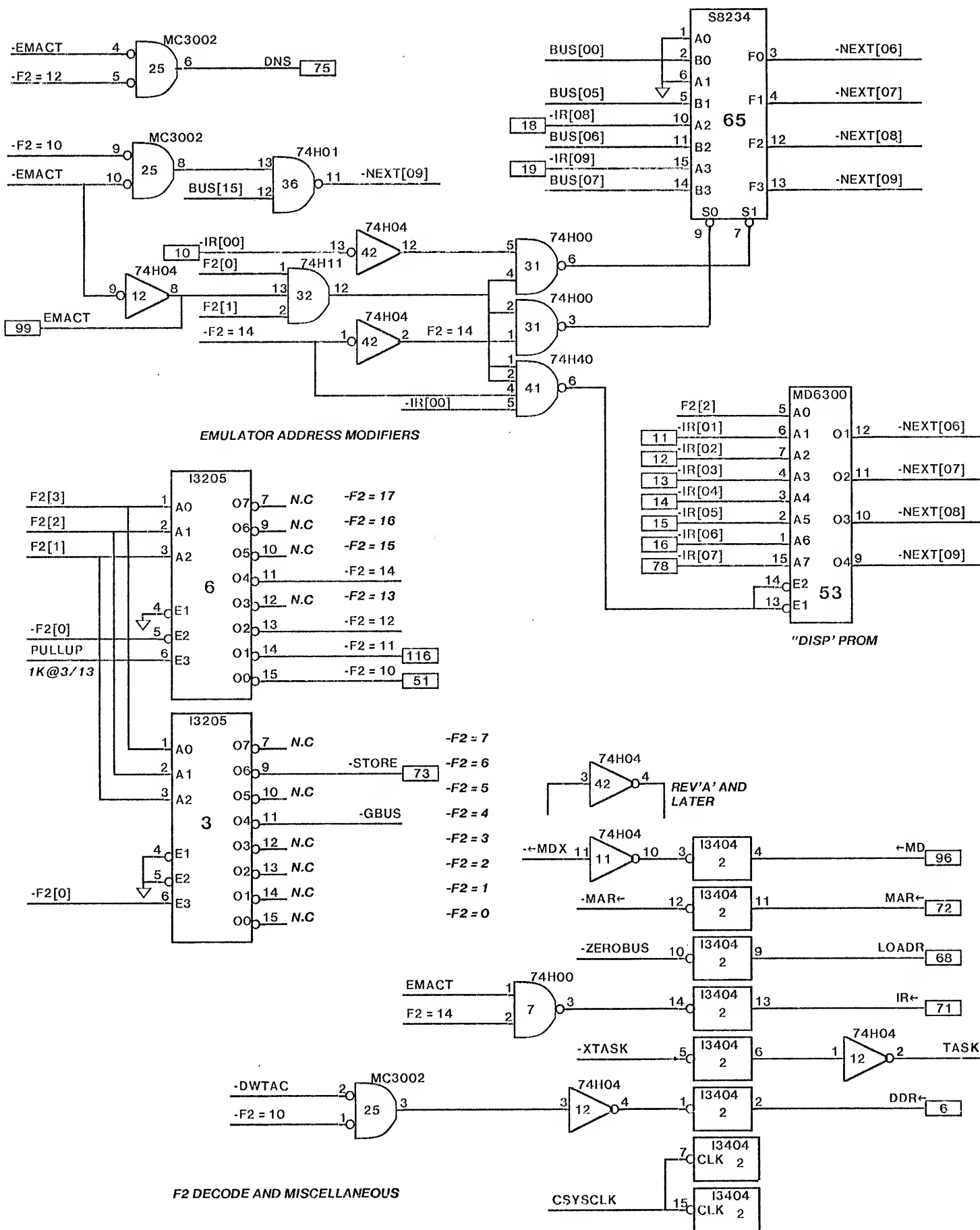
PC RAM

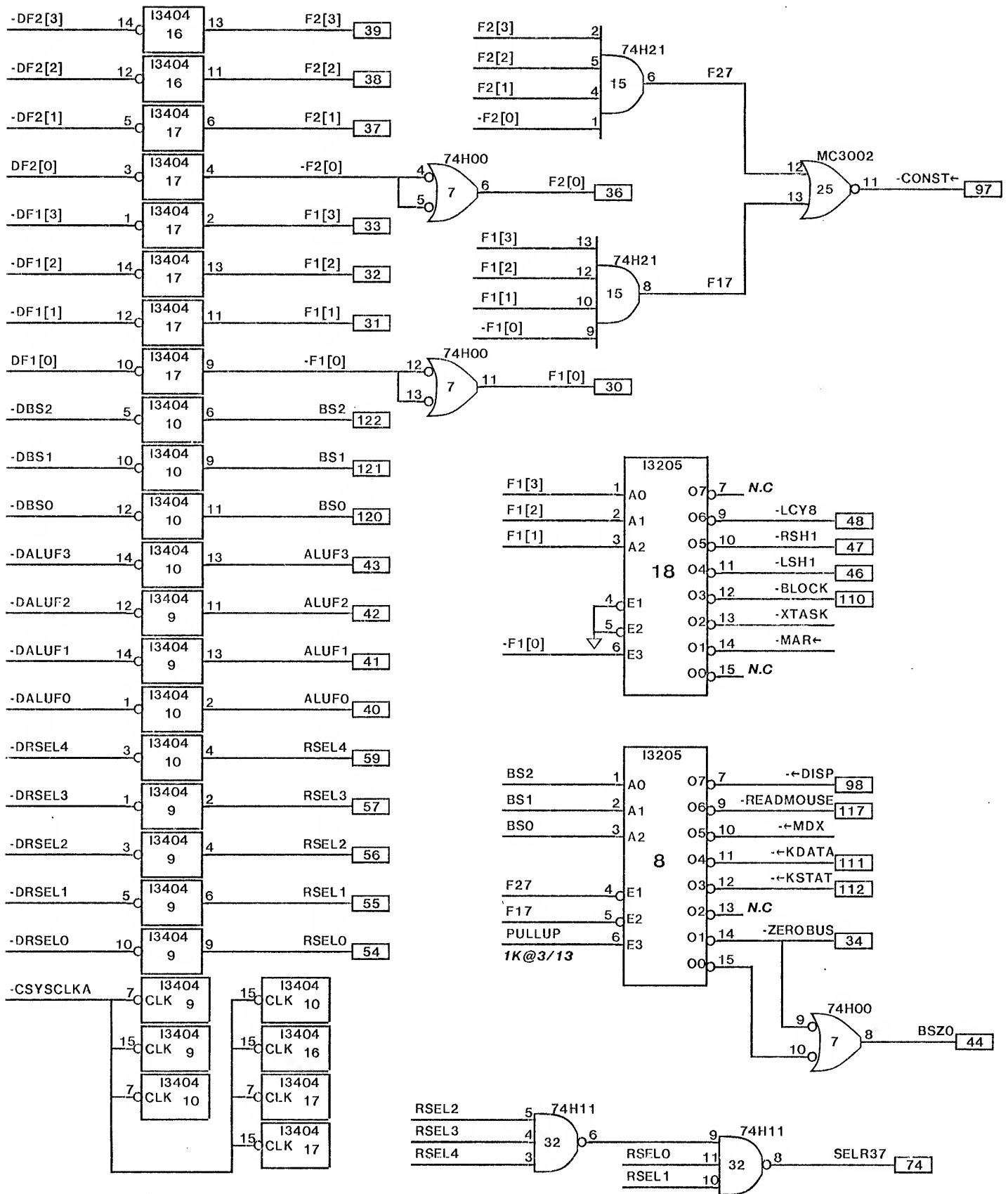




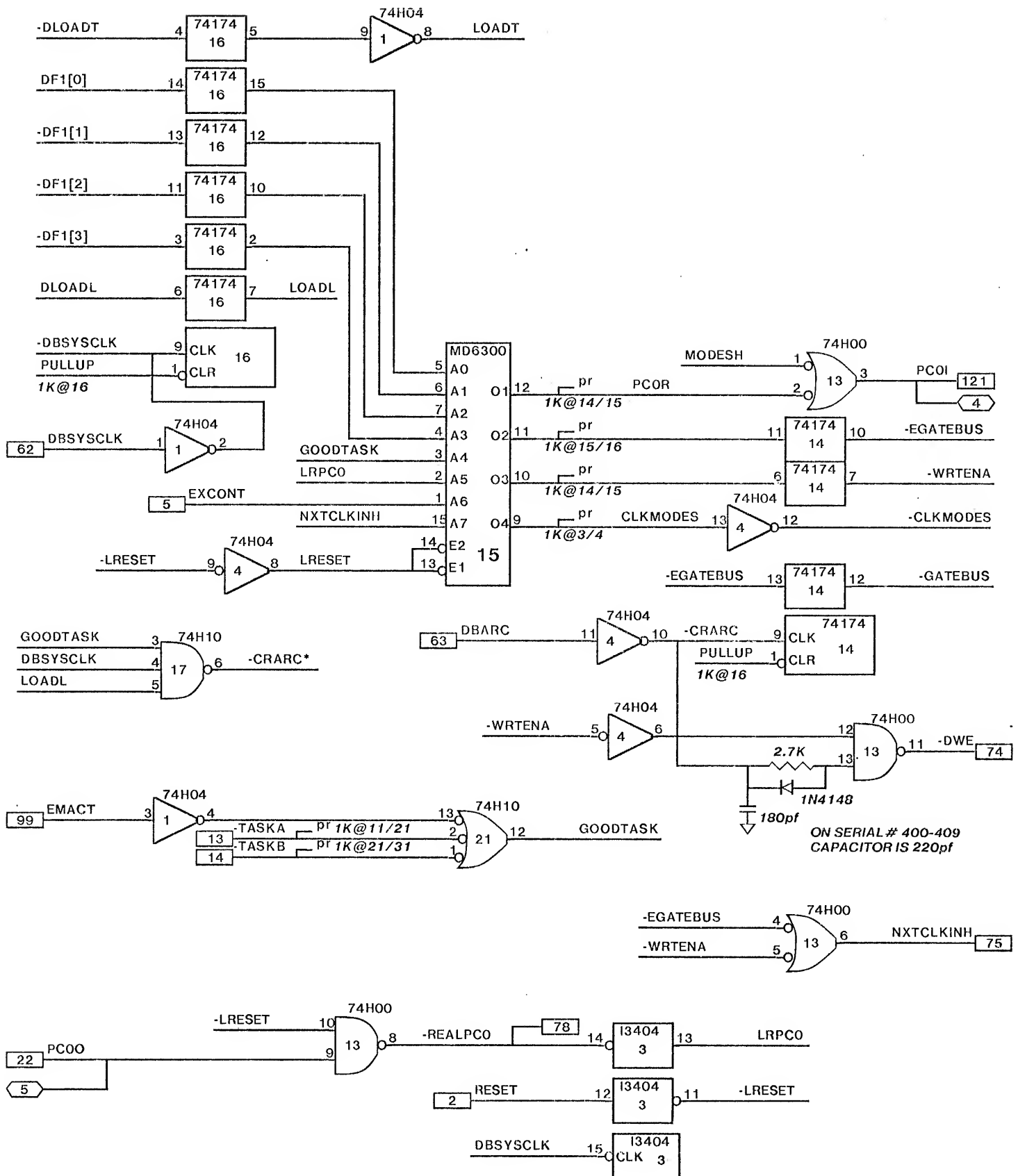


CONTROL Page 6





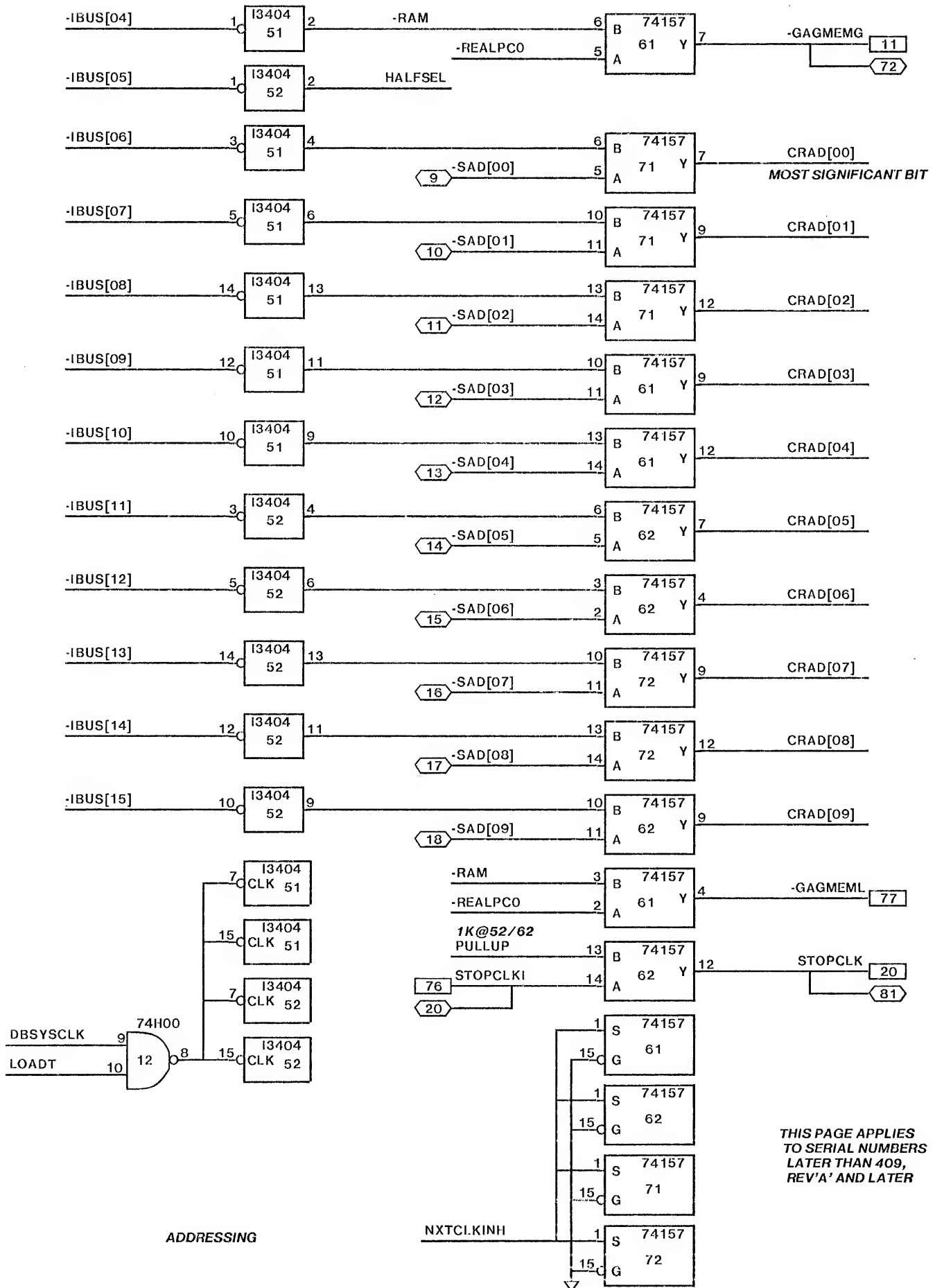
MIR, F1 AND DECODE

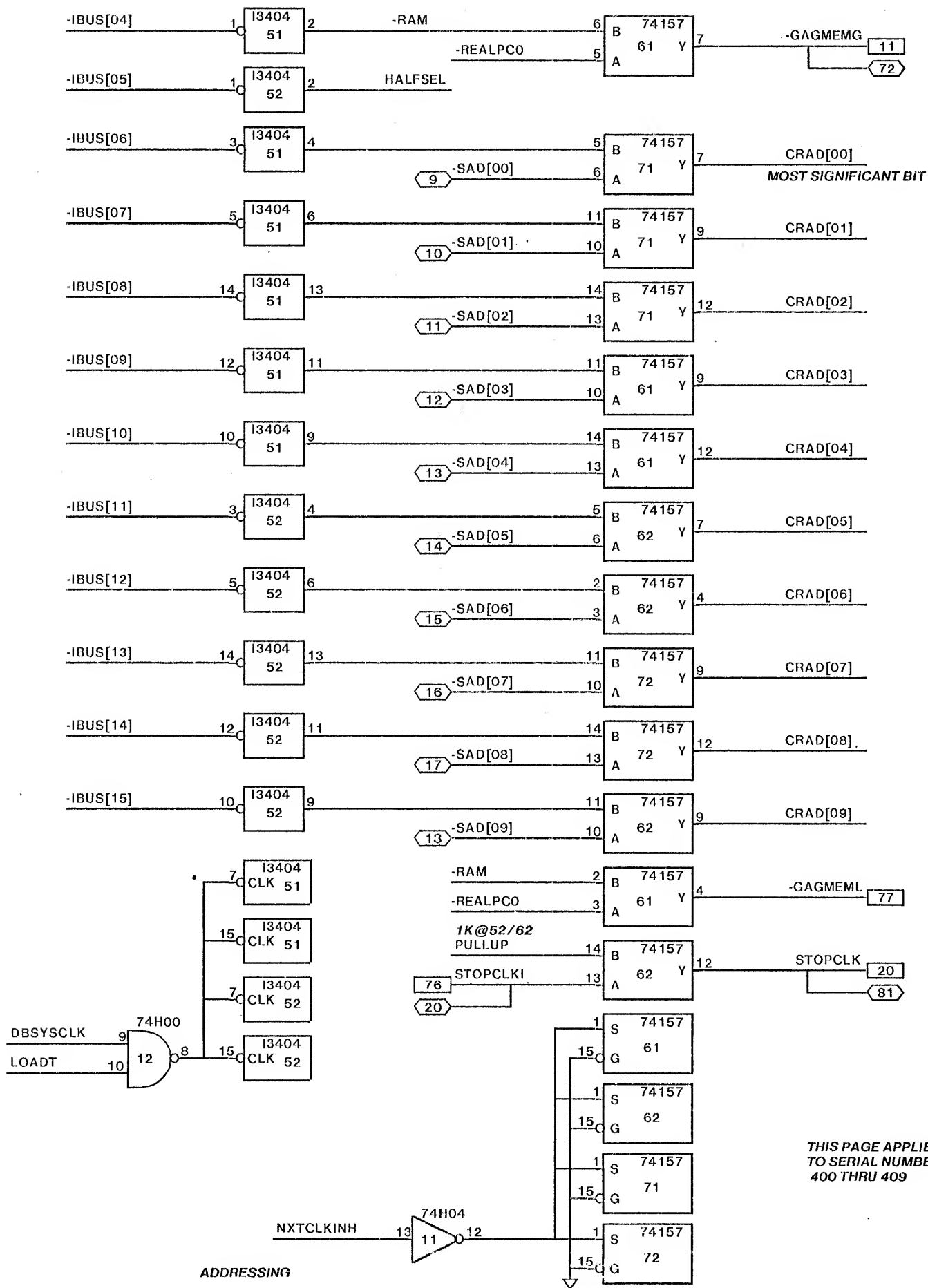


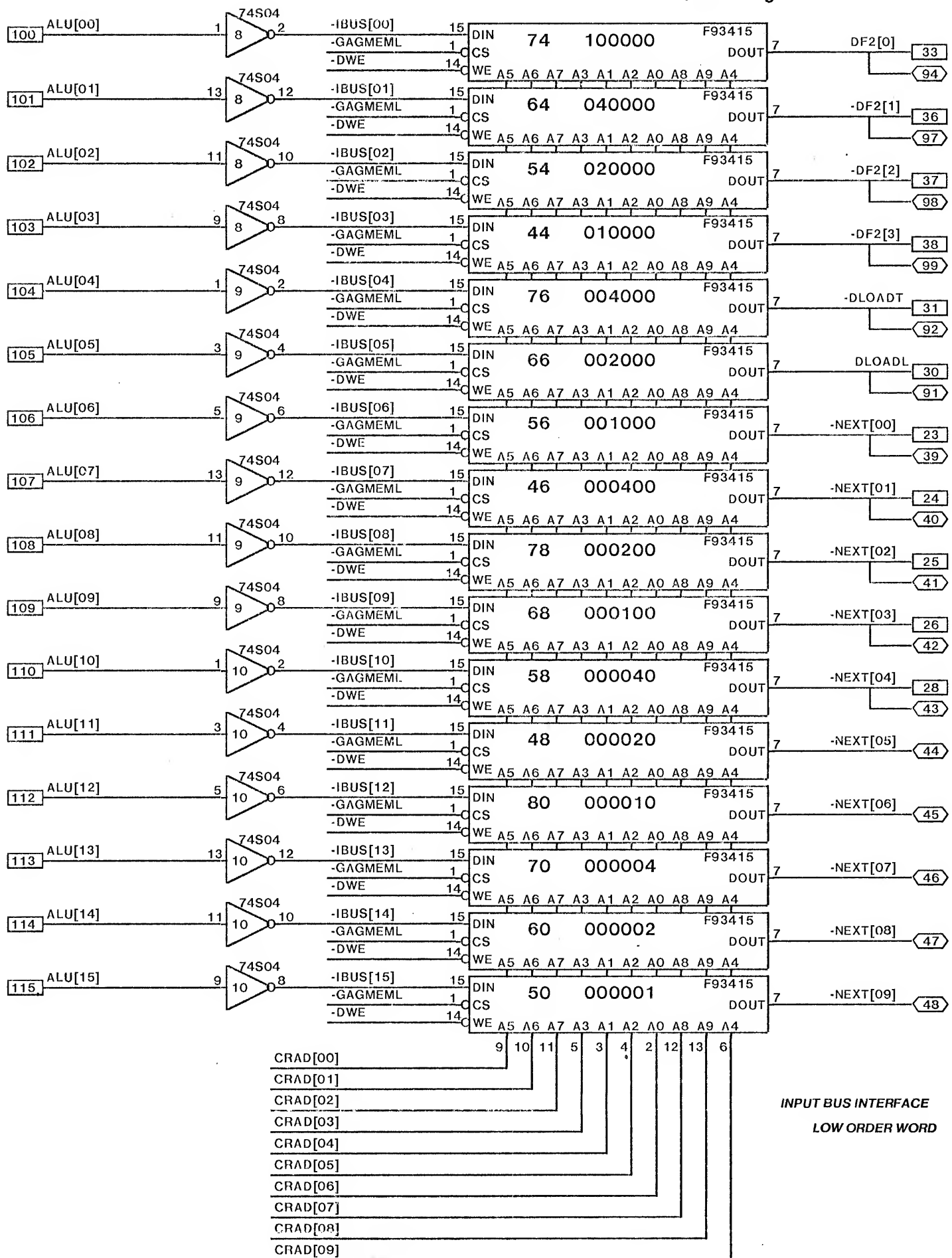
CONTROL SIGNALS

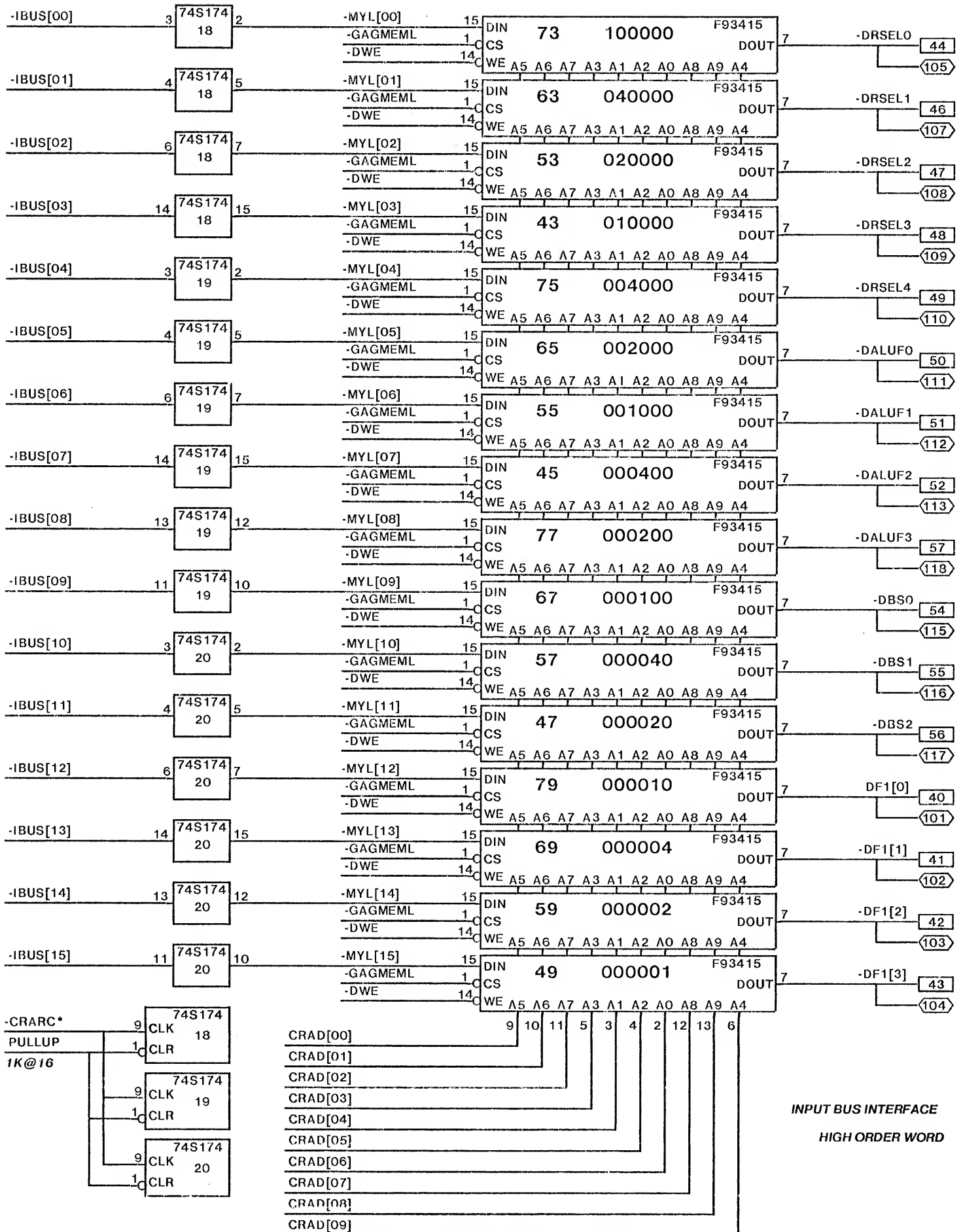




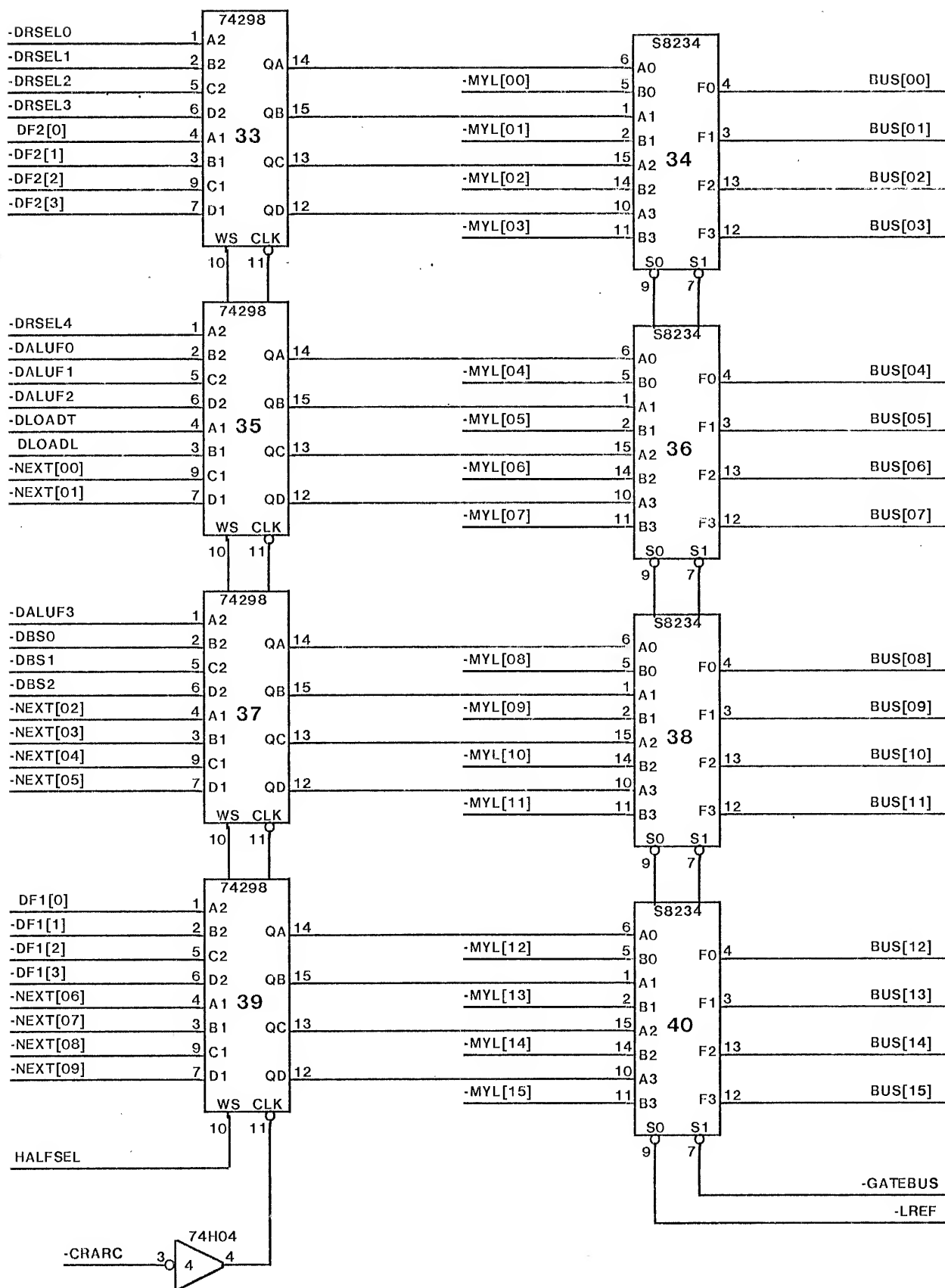




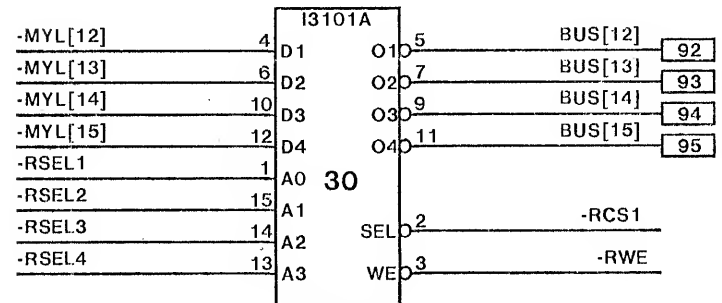
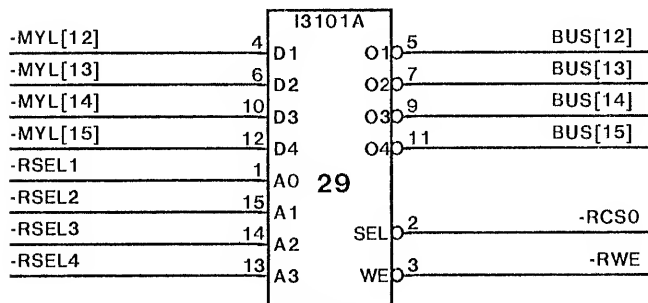
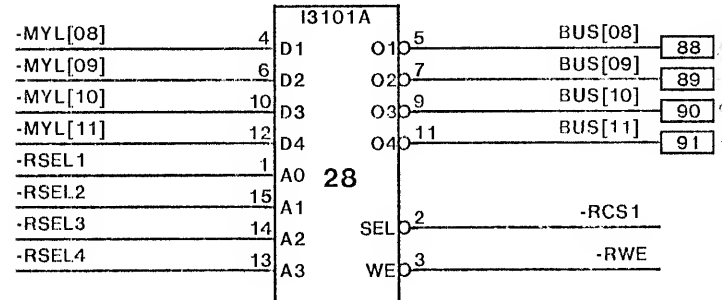
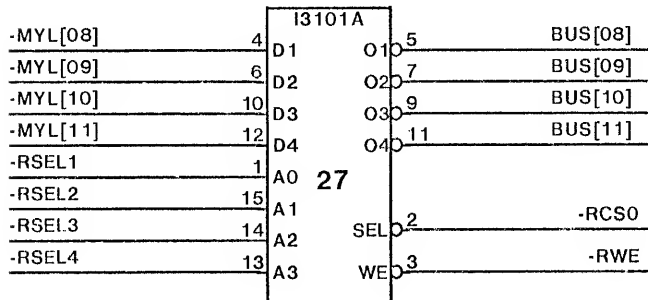
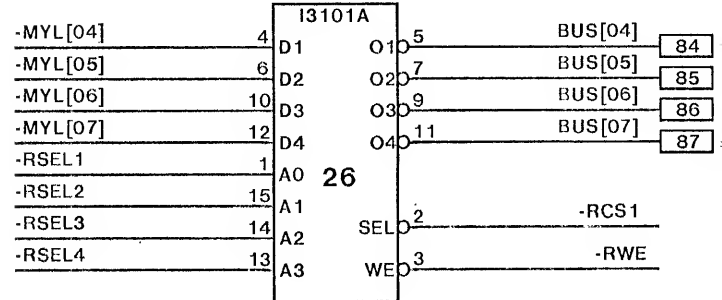
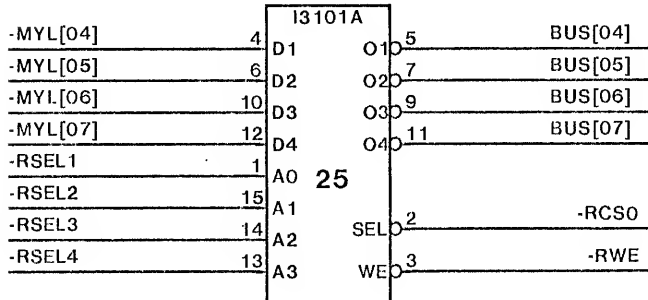
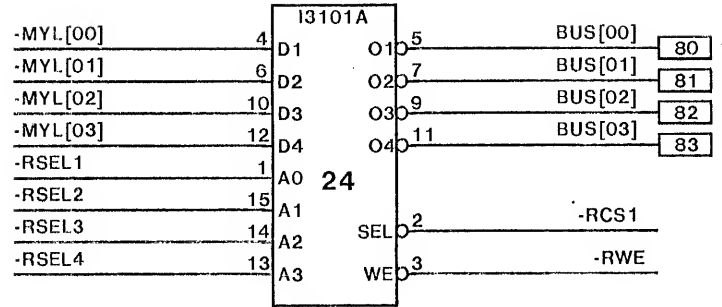
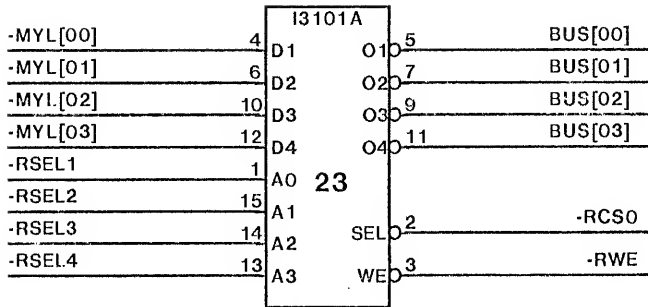




CRAM Page 6



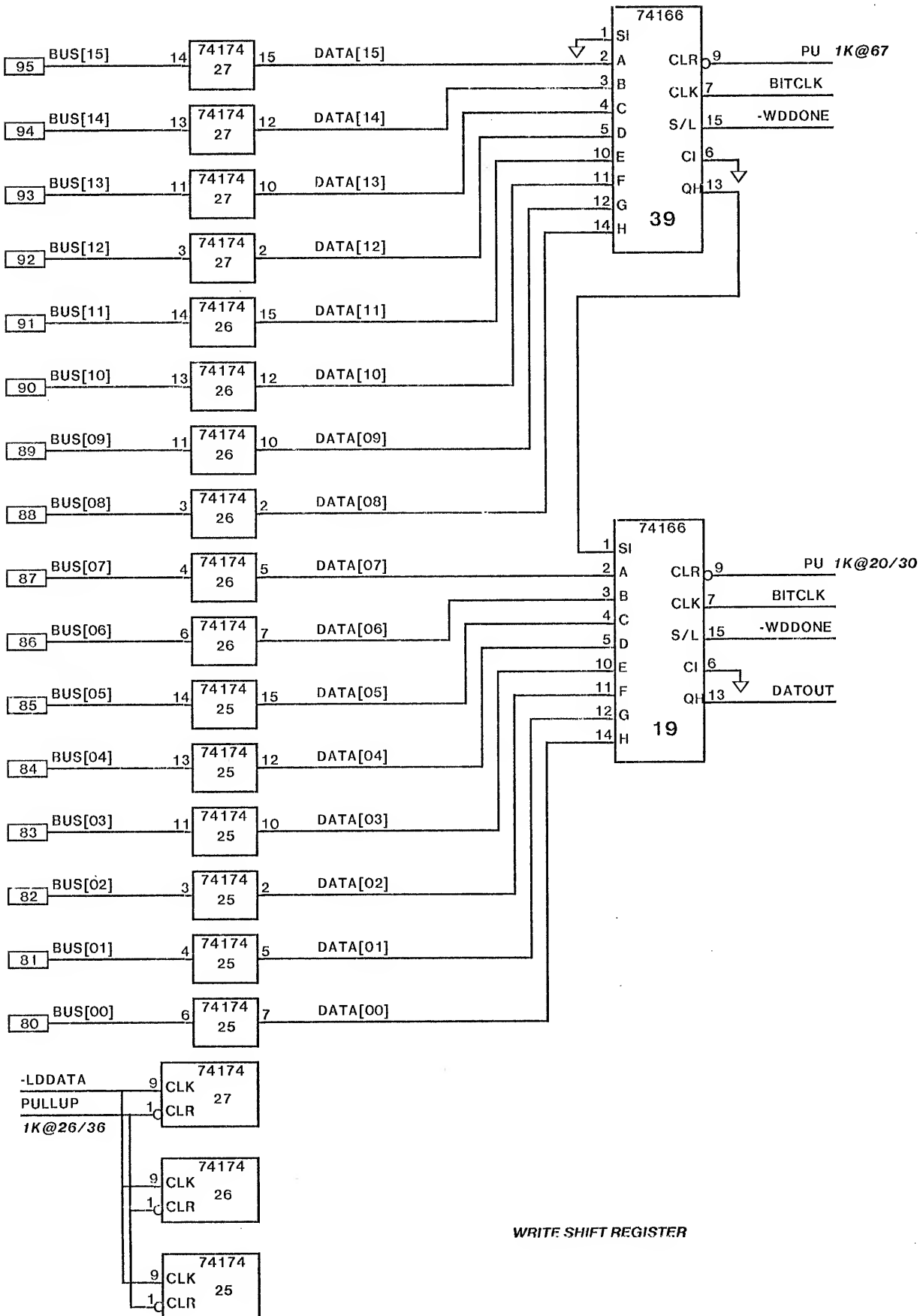
## OUTPUT BUS INTERFACE



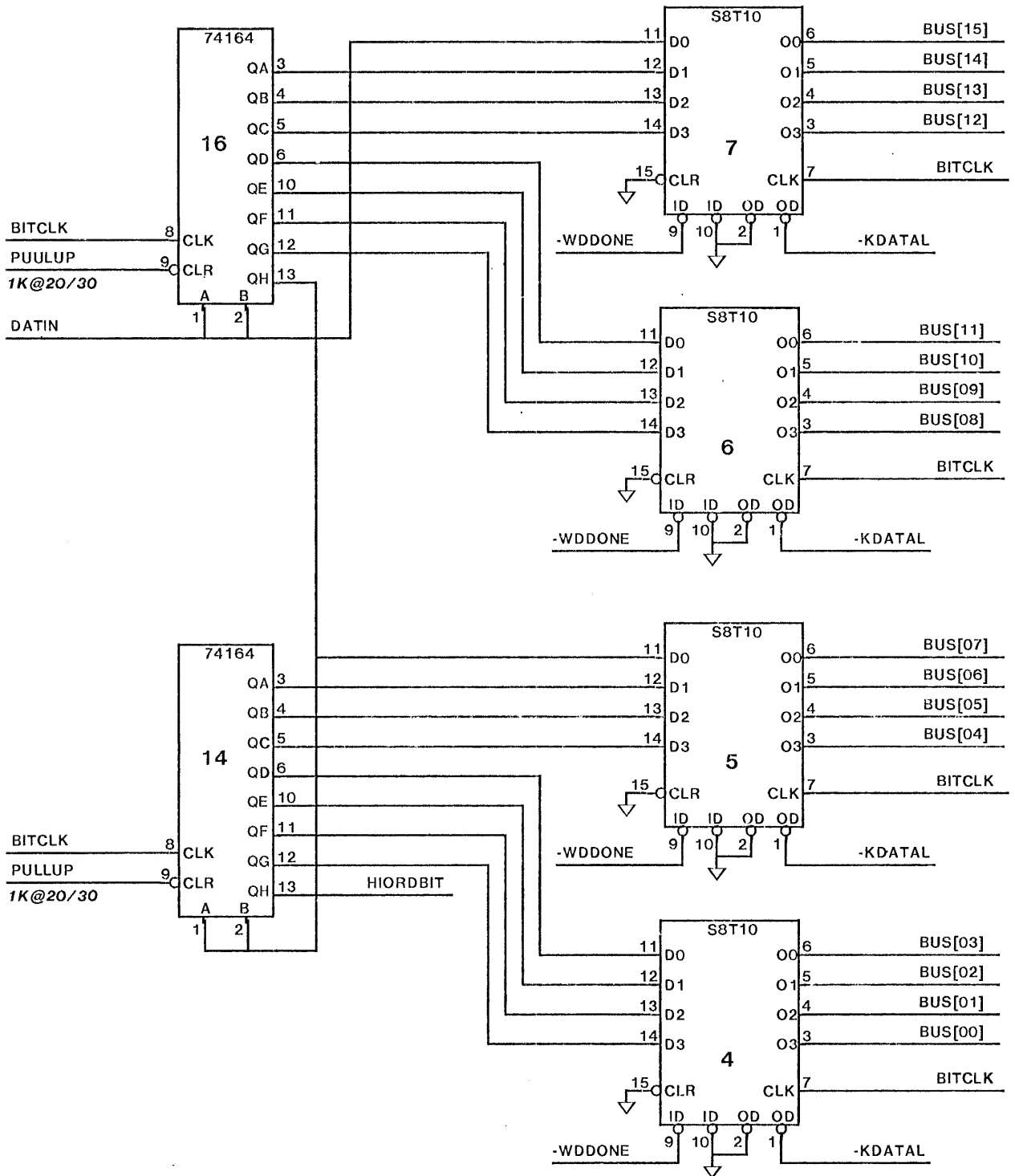
(41-57)

(60-77)

'R' REGISTERS

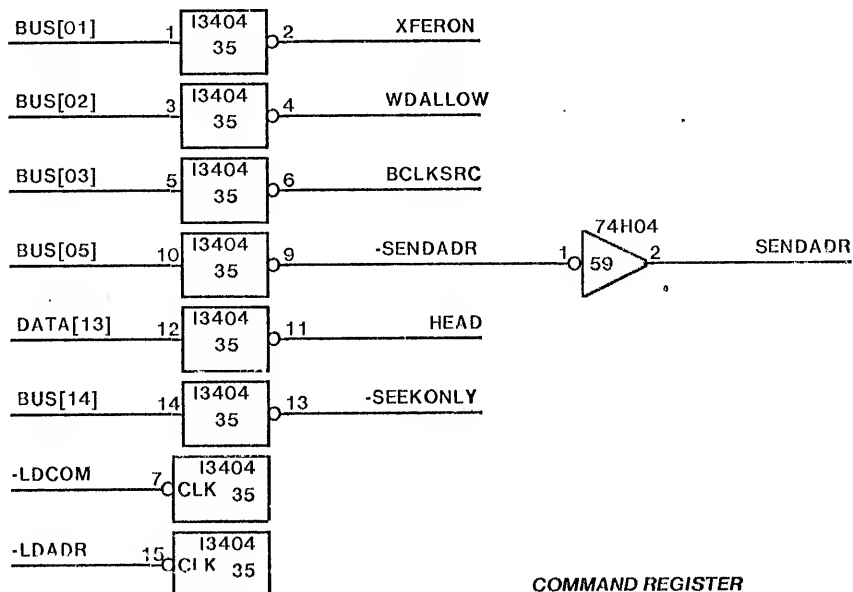
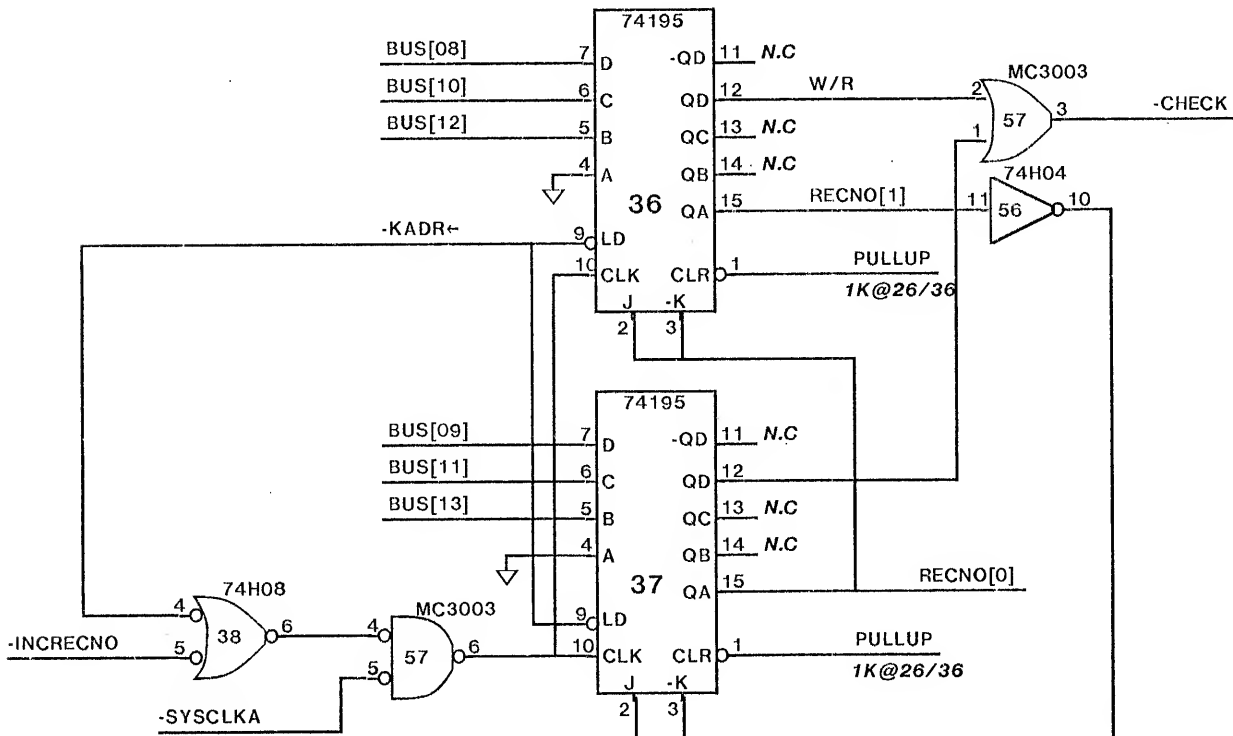
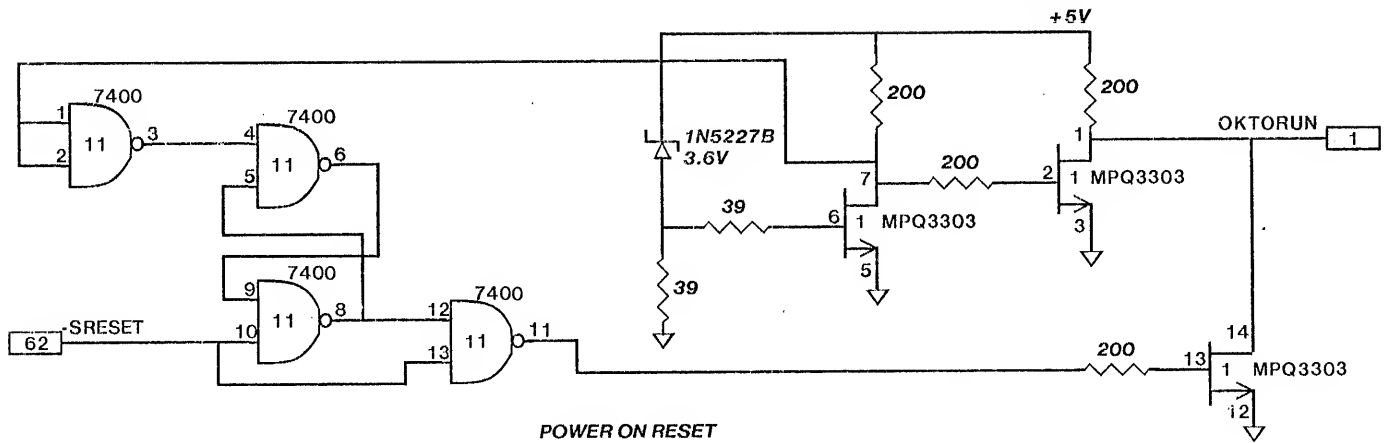




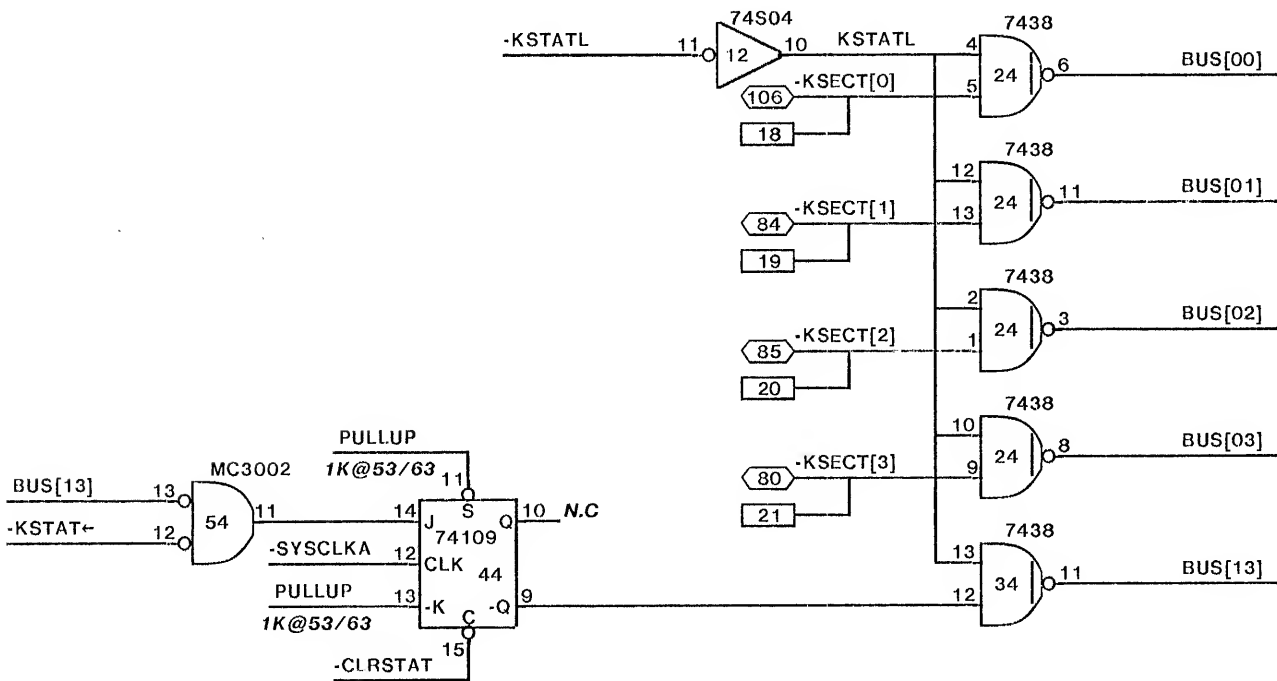
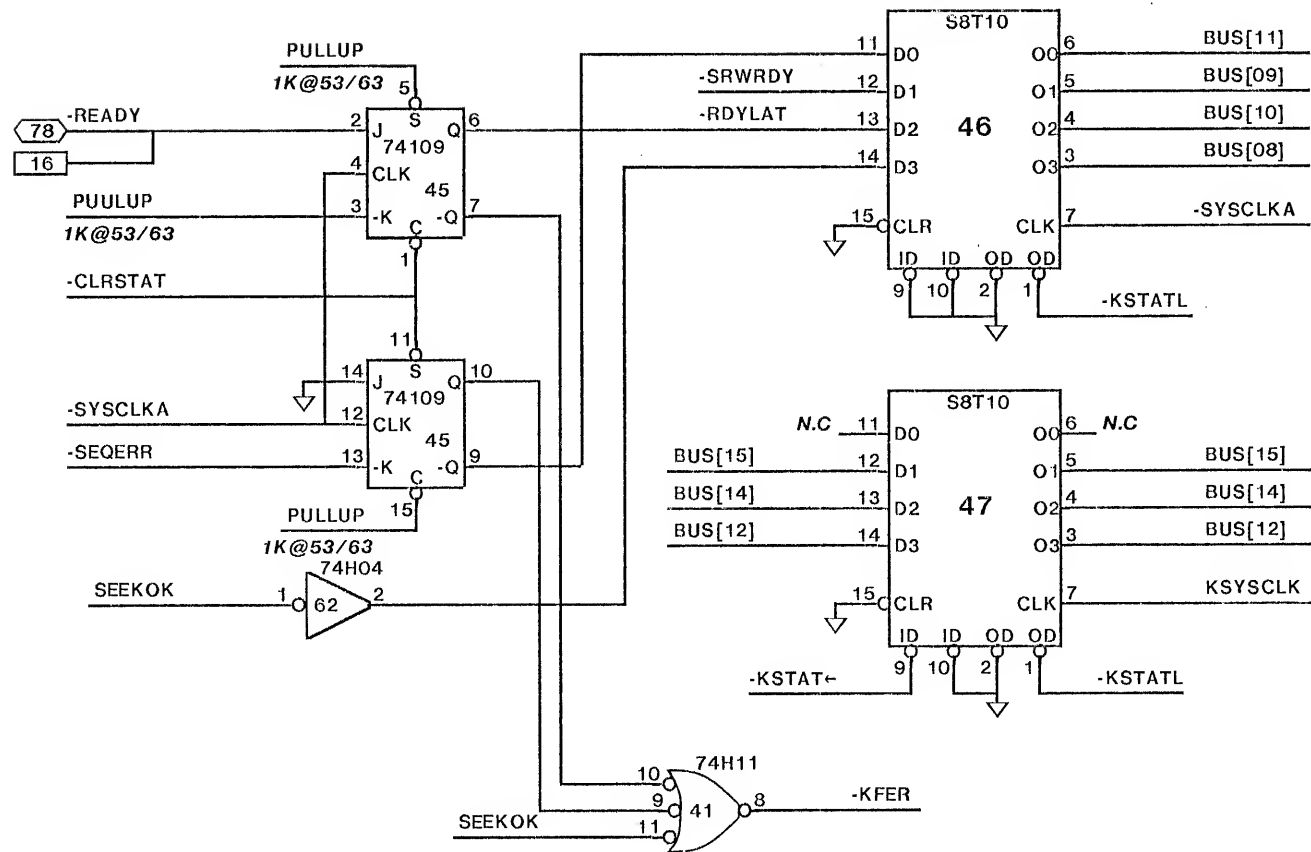


READ SHIFT REGISTER

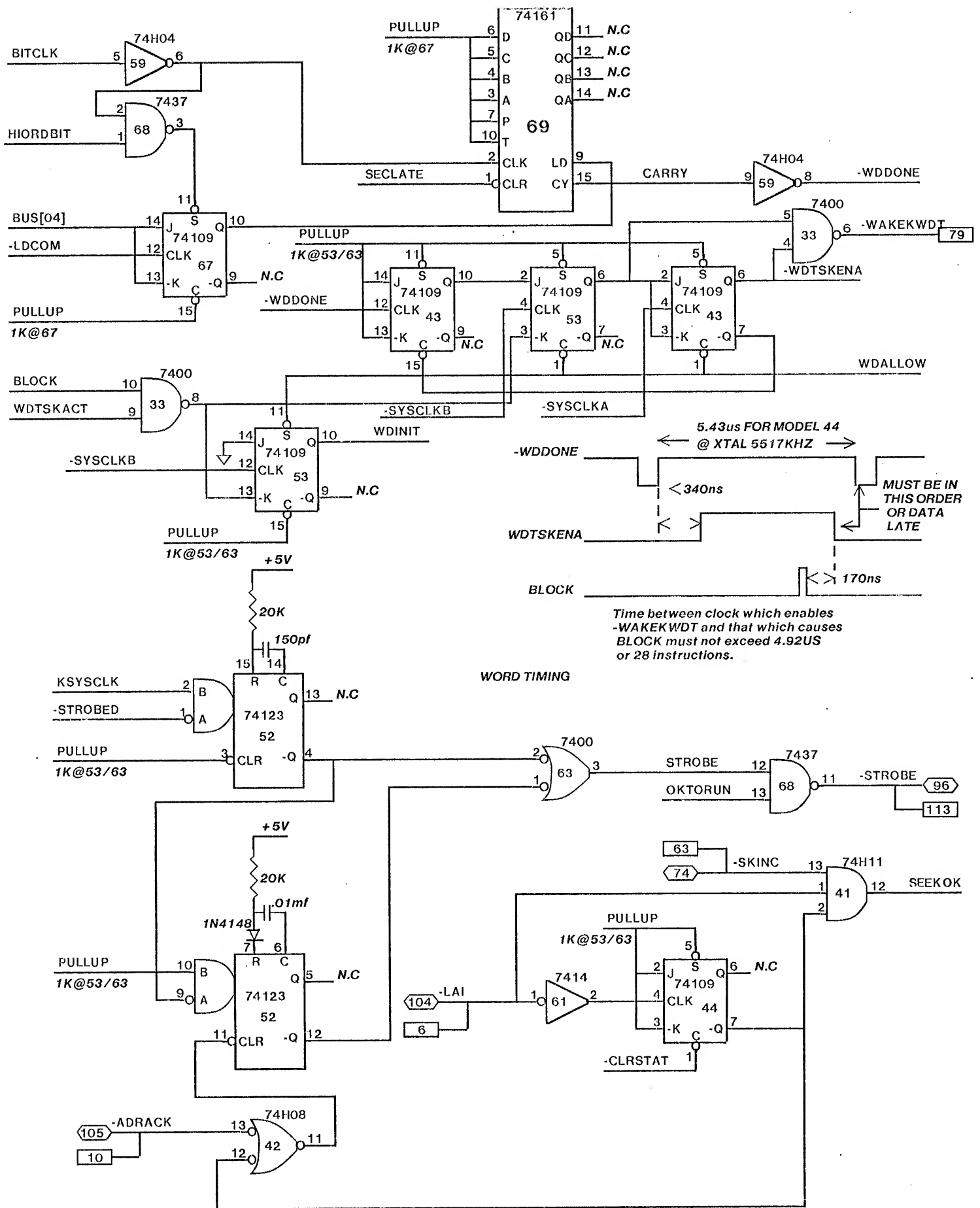
DISK CONTROLLER Page 3

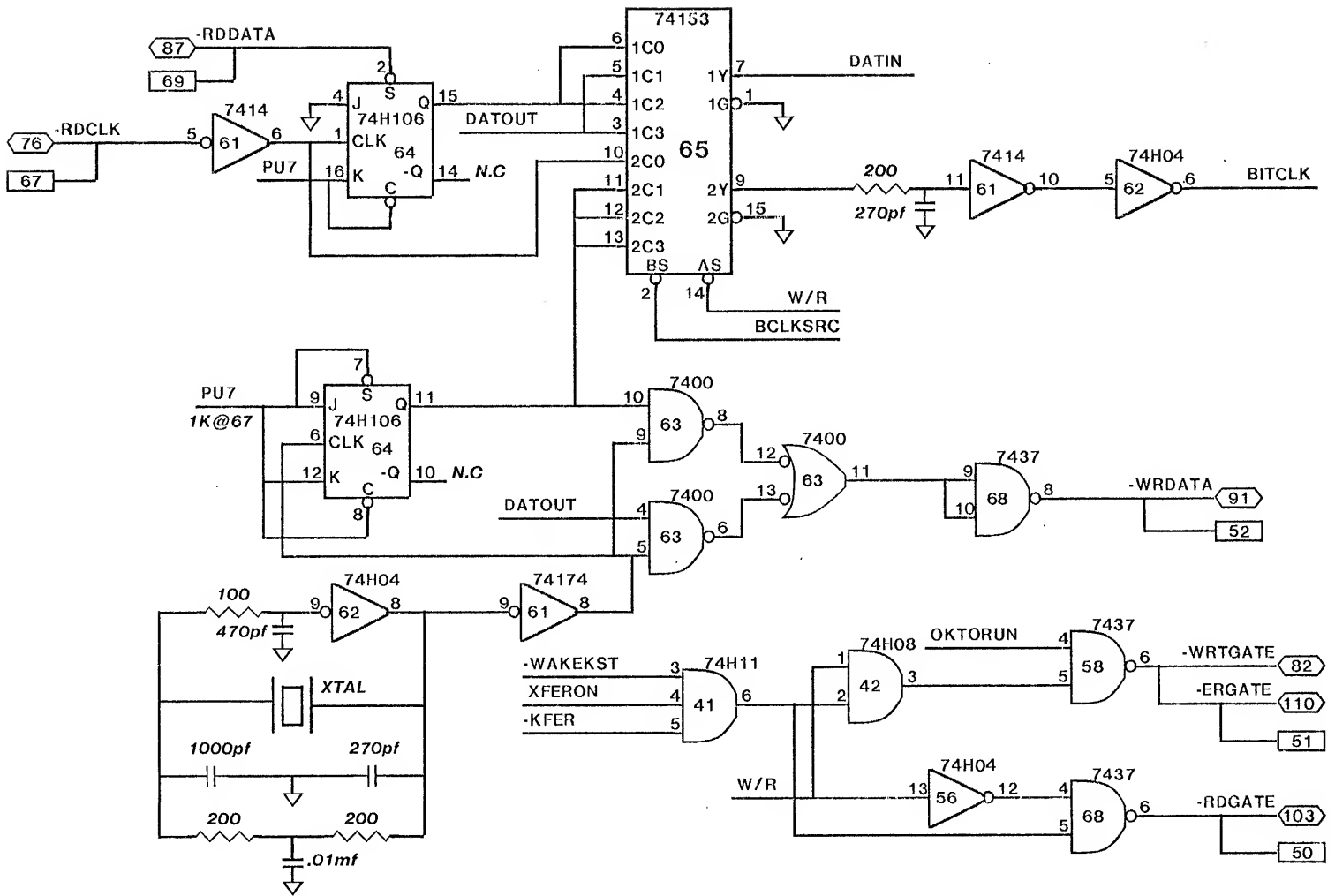


### COMMAND REGISTER

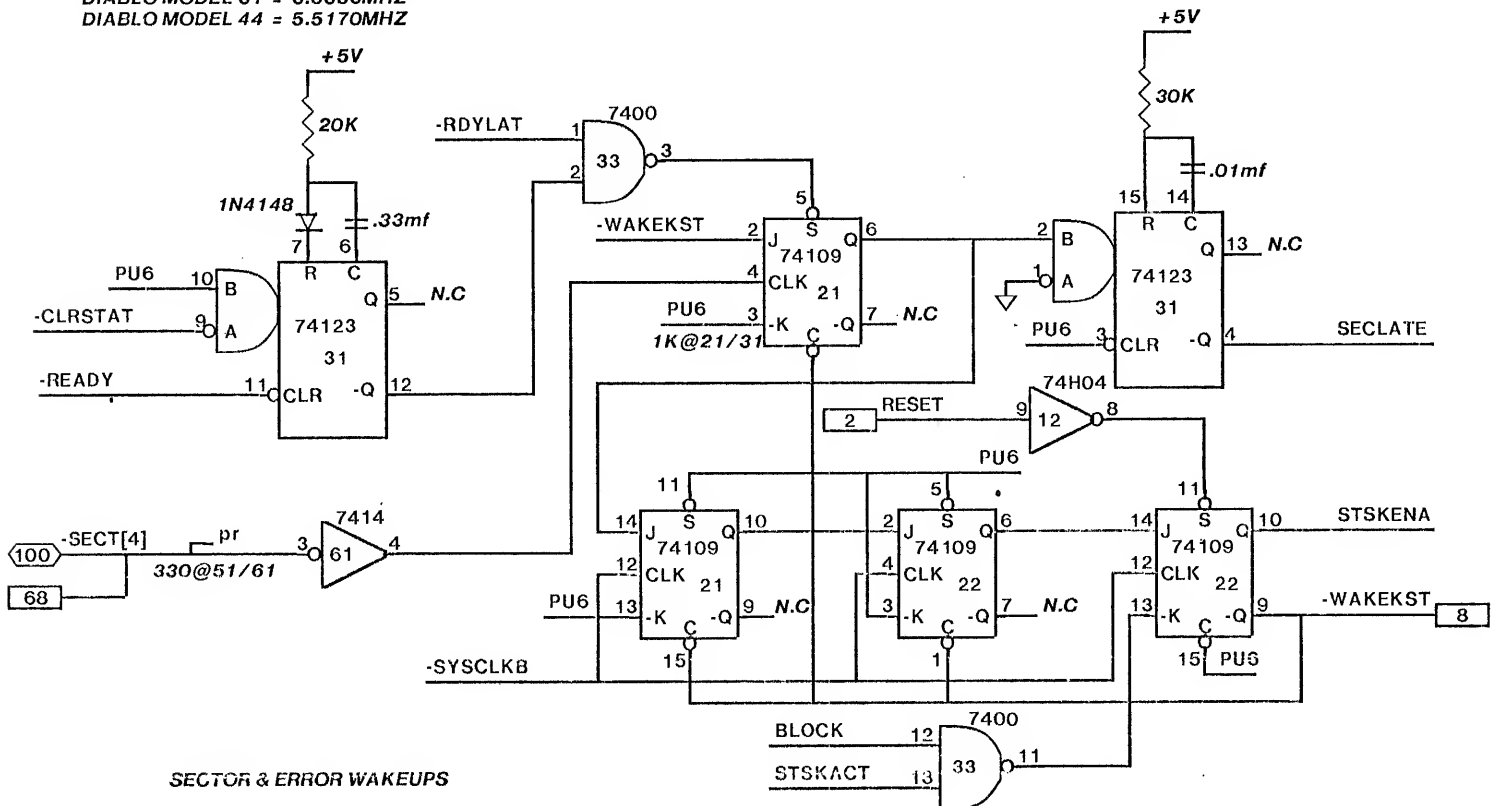


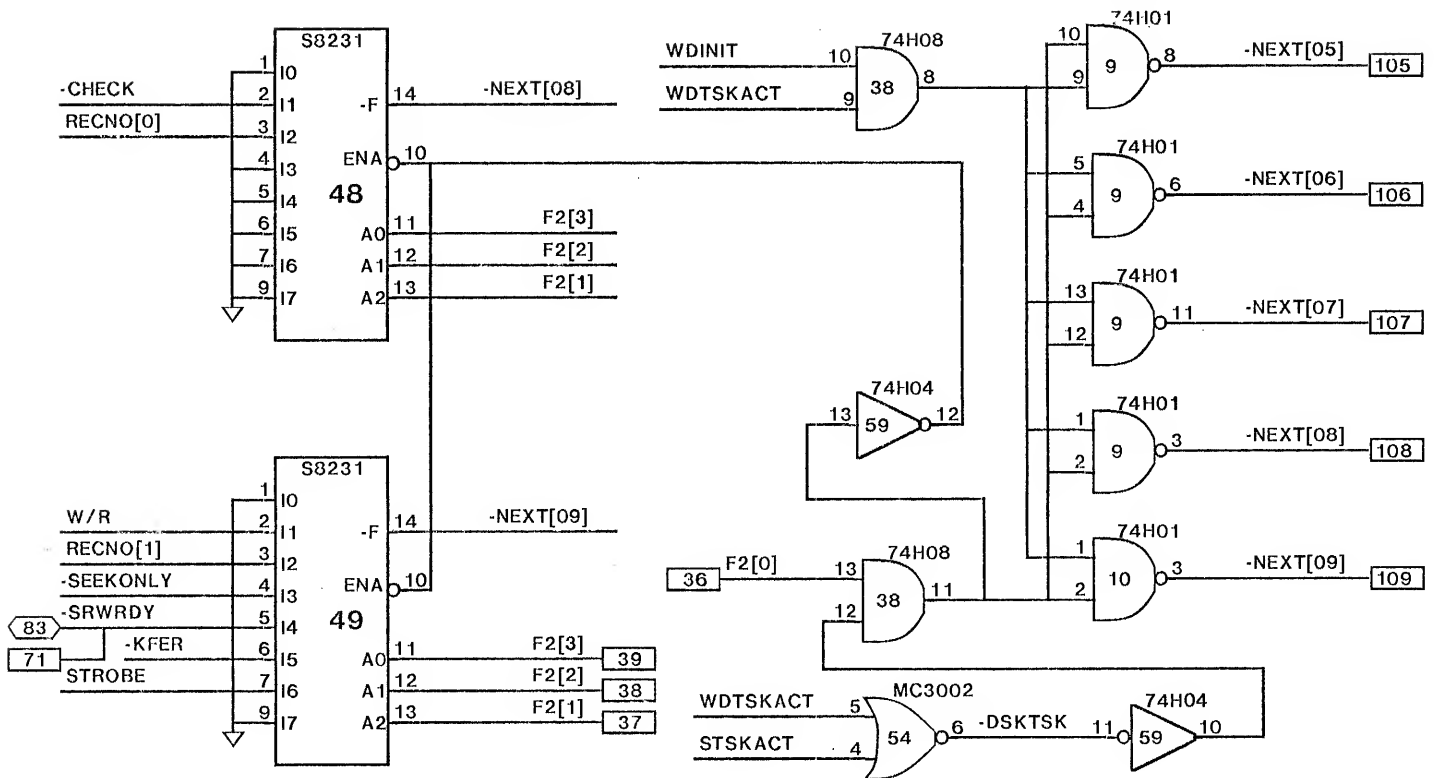
STATUS



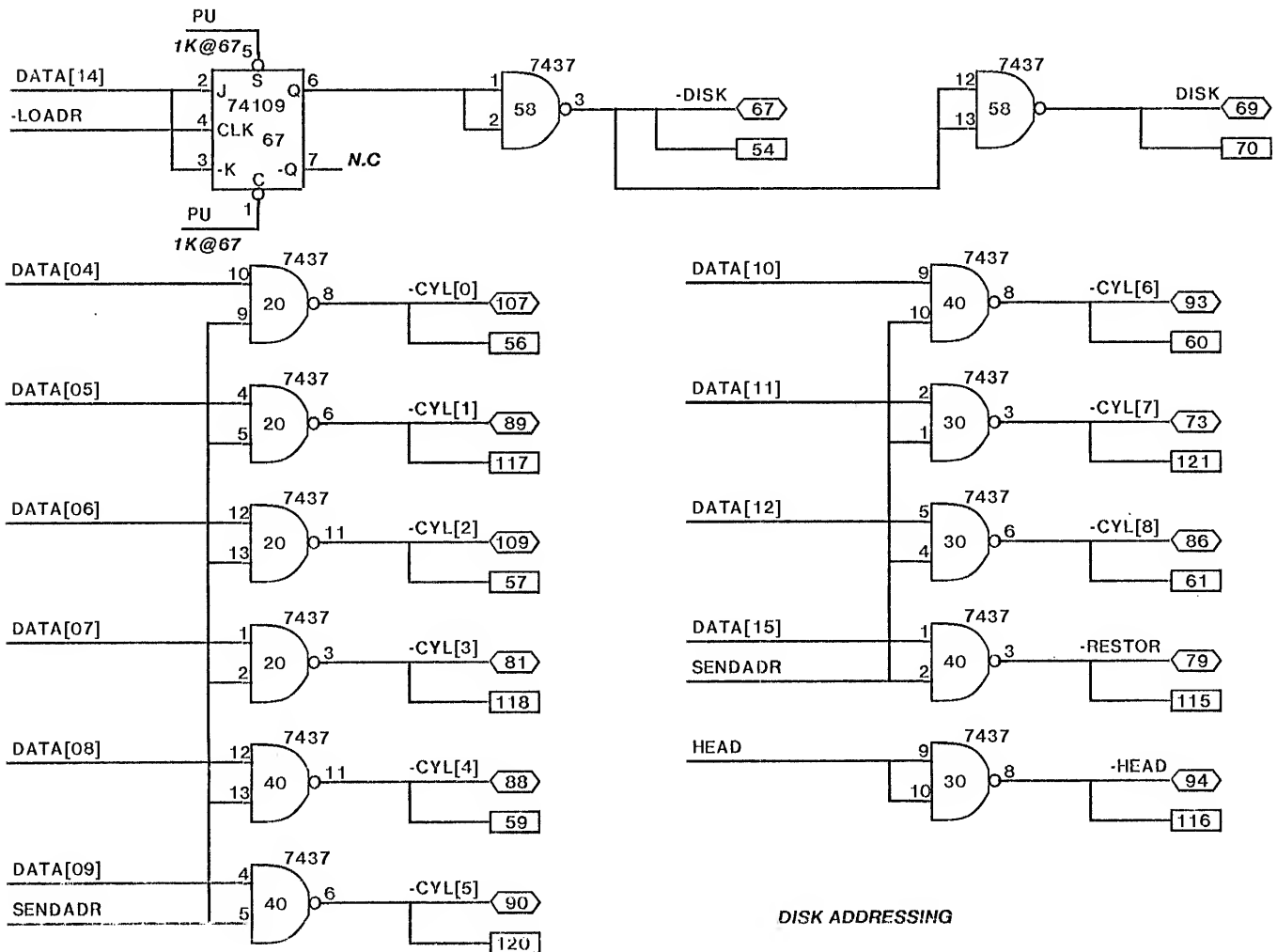


## DATA HANDLING

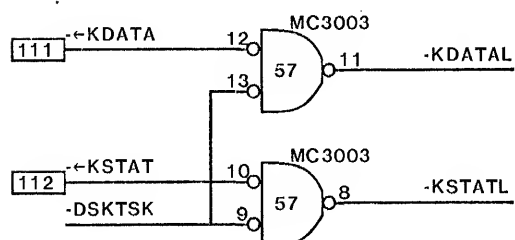
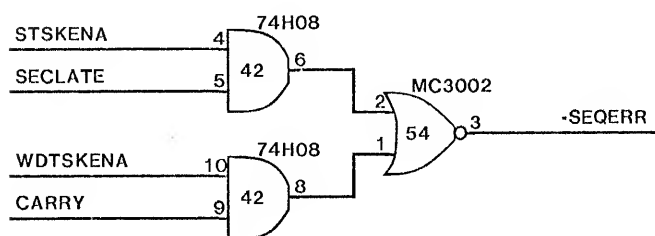
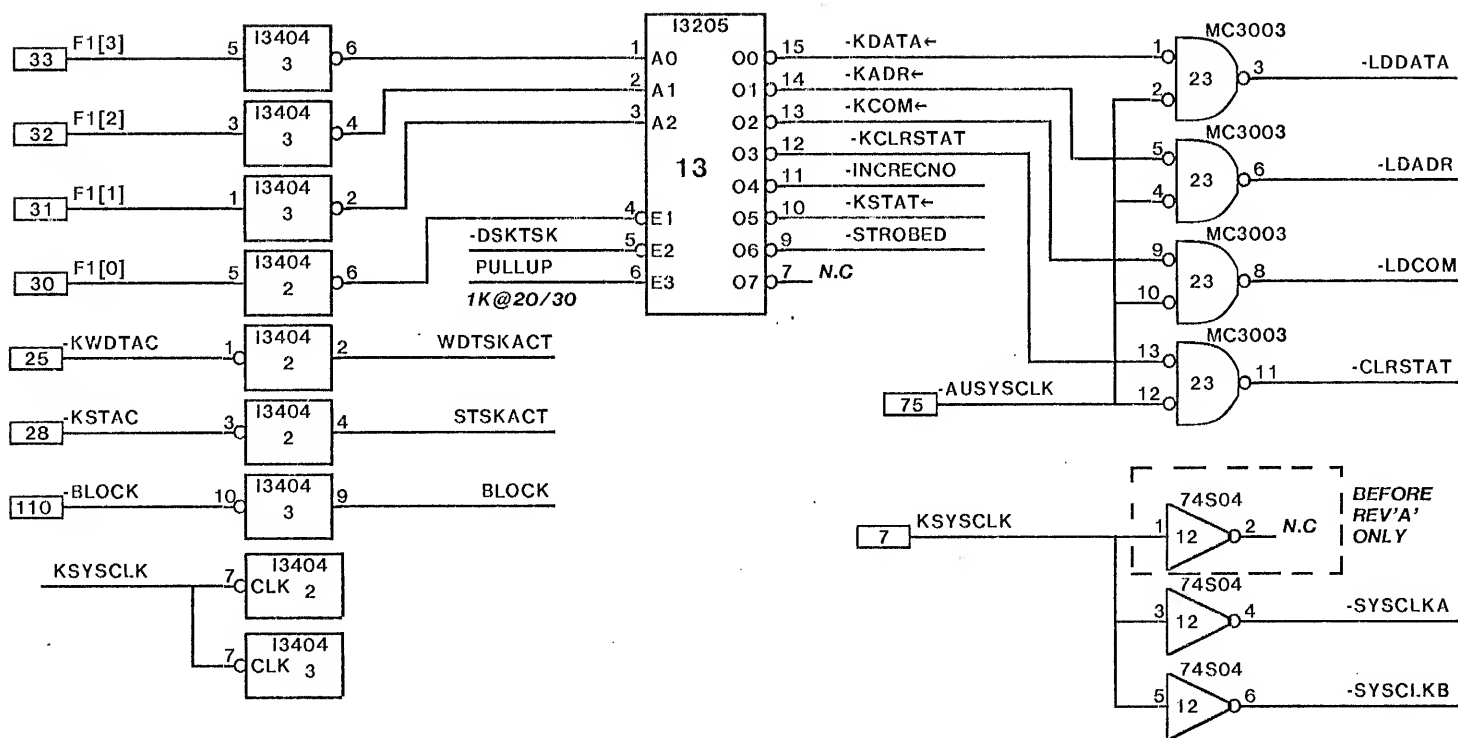




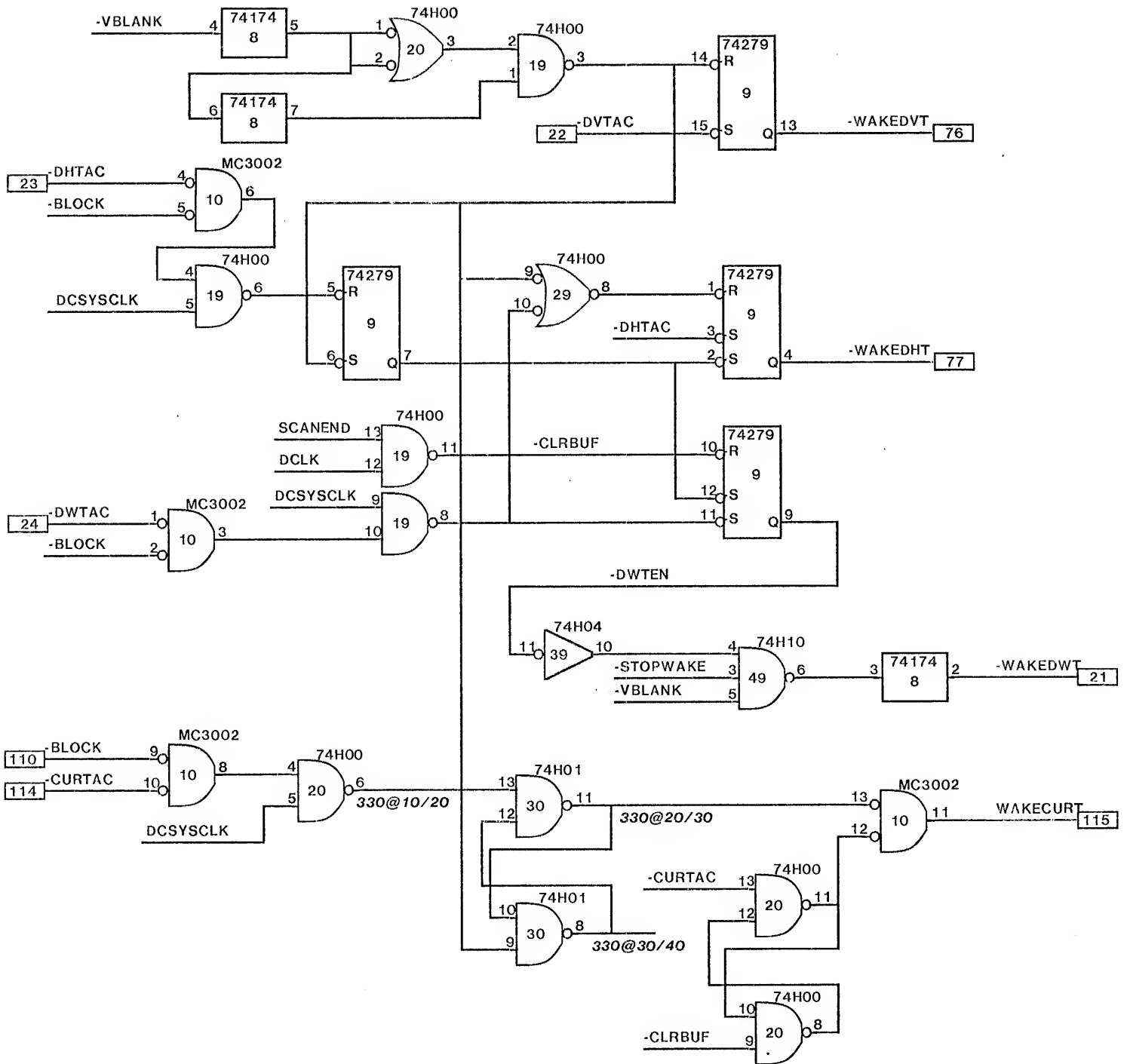
## ADDRESS MODIFIERS



## DISK ADDRESSING

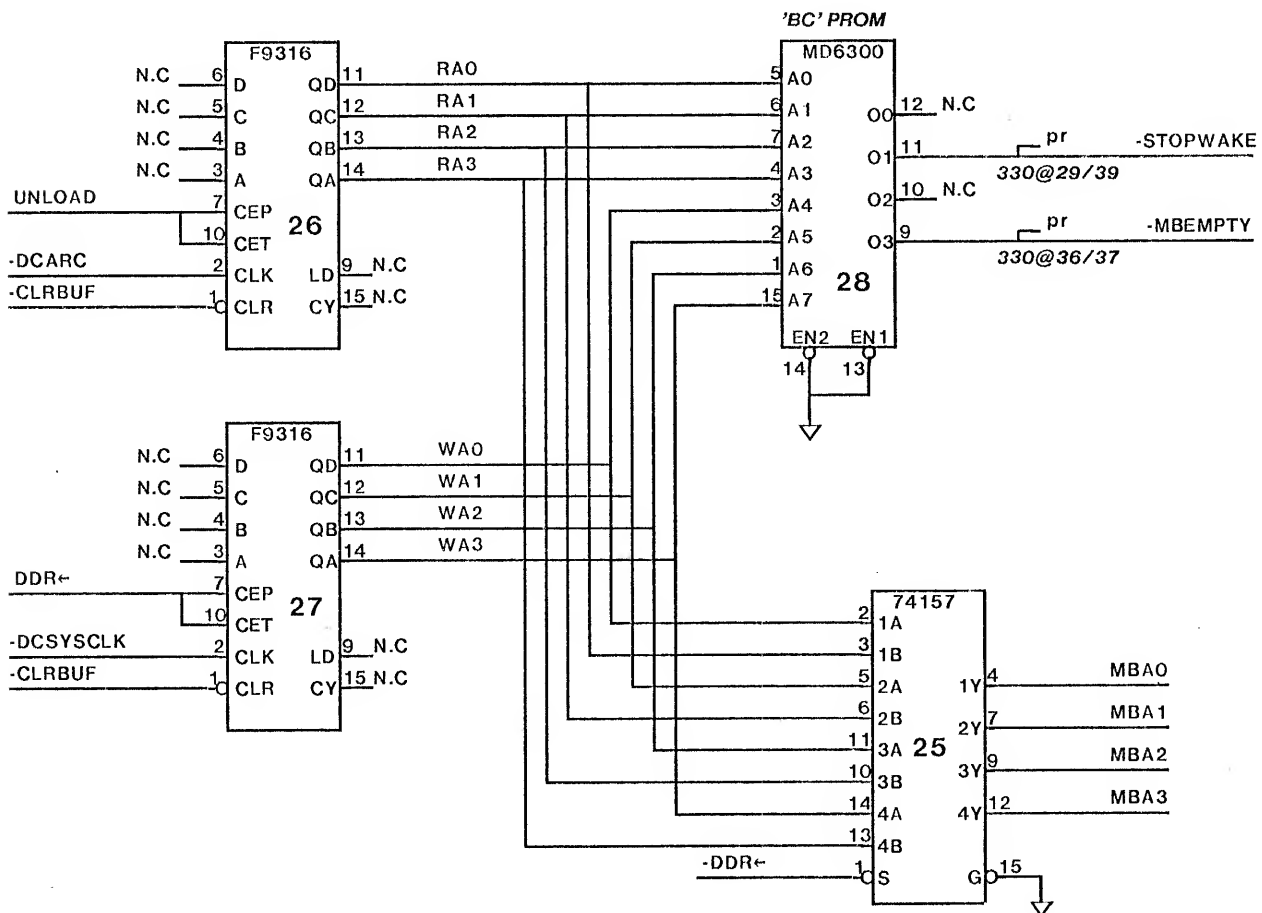
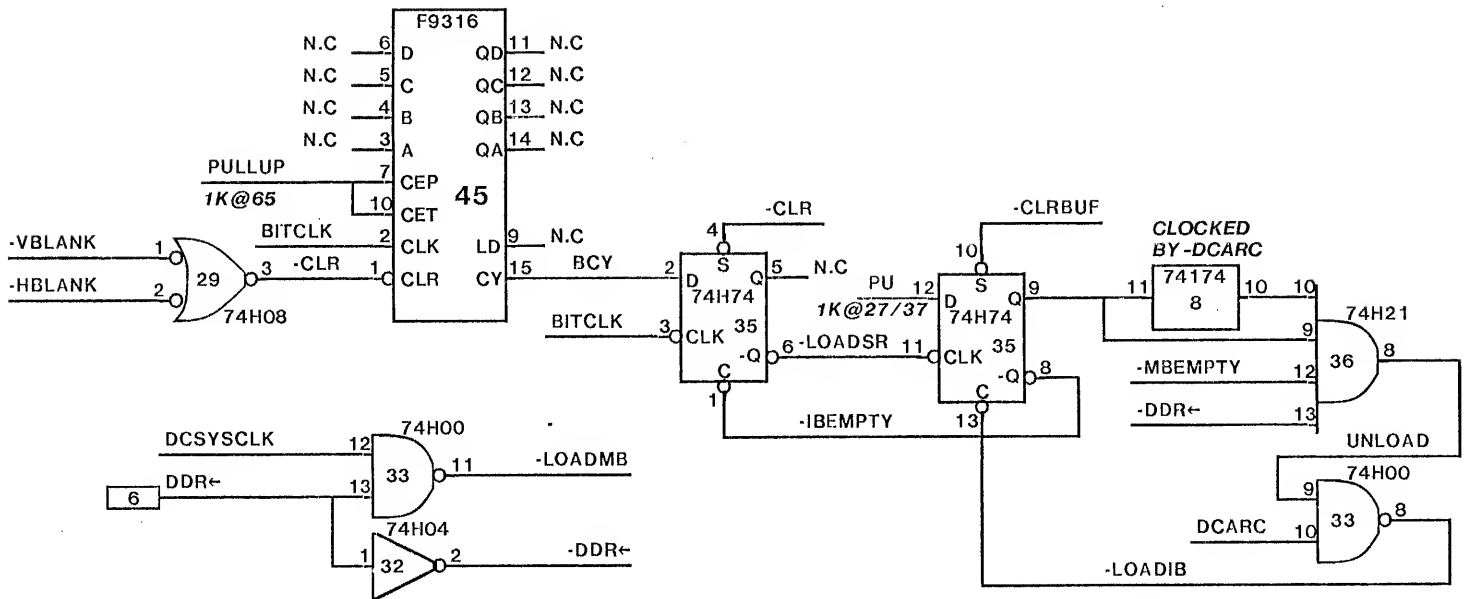


## F DECODE AND CLOCKS

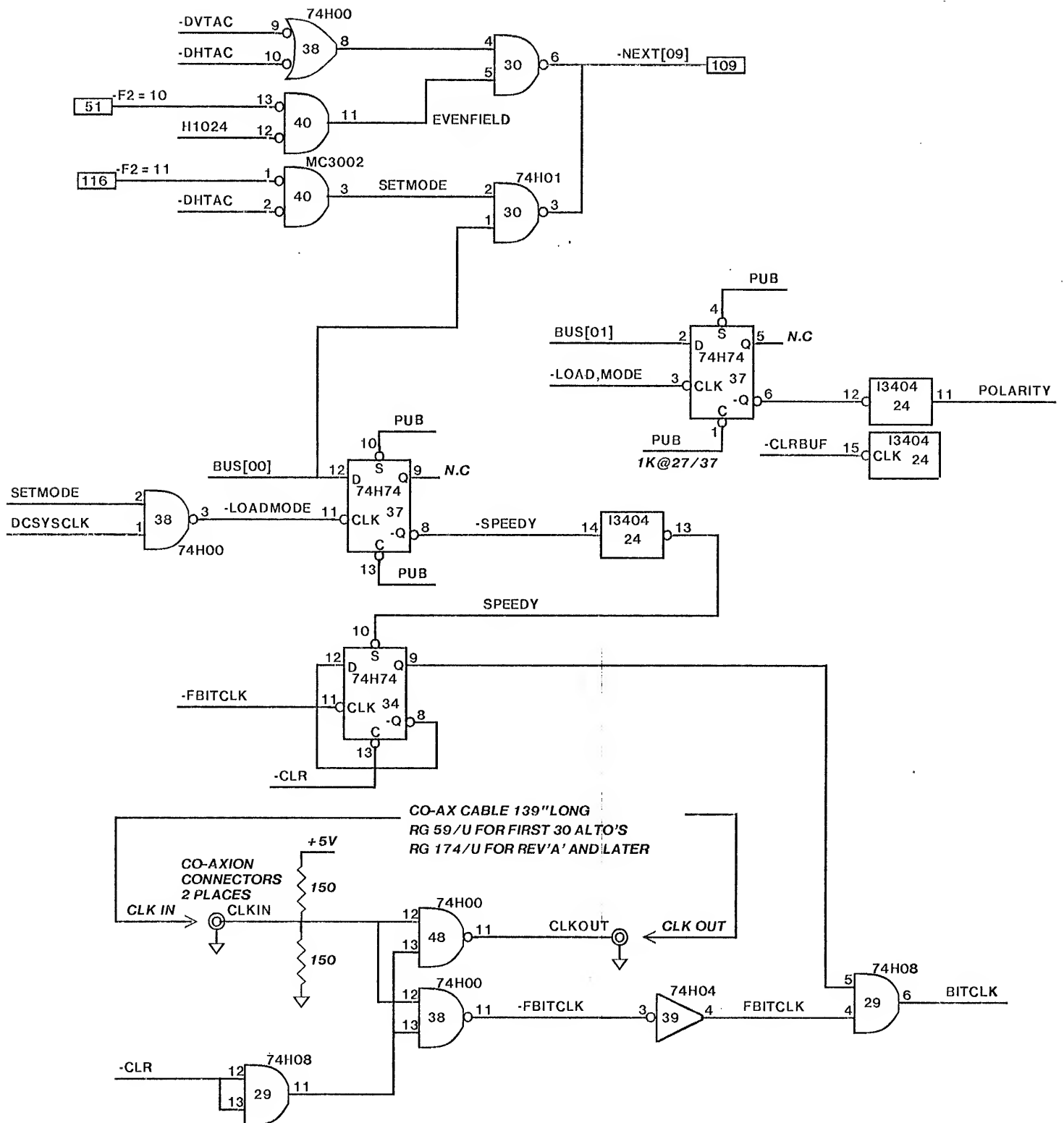


WAKEUPS

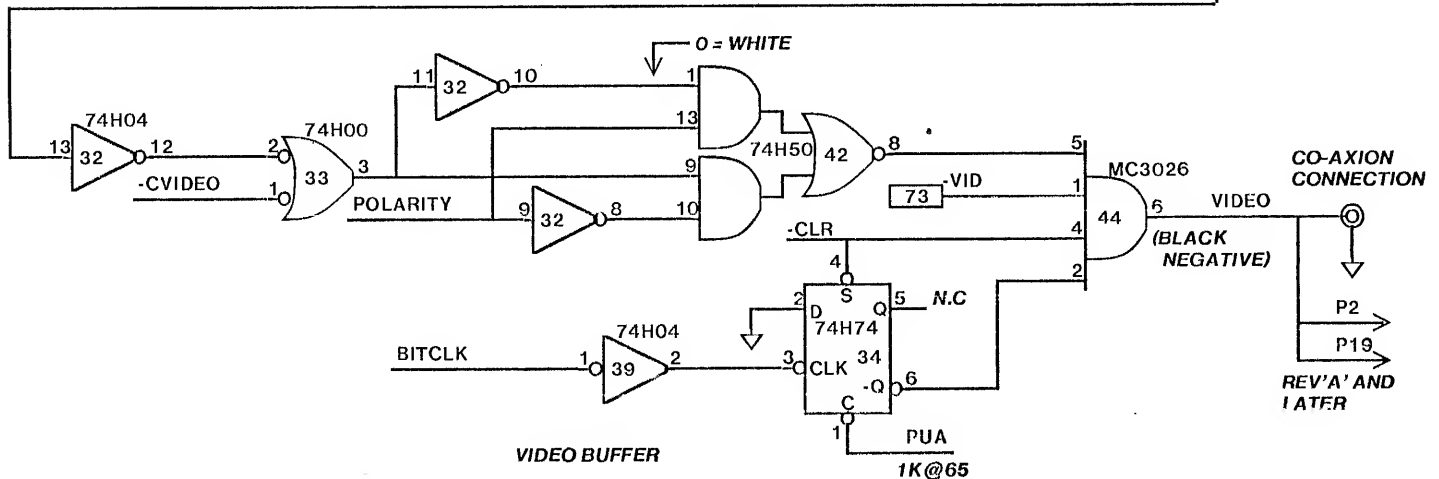
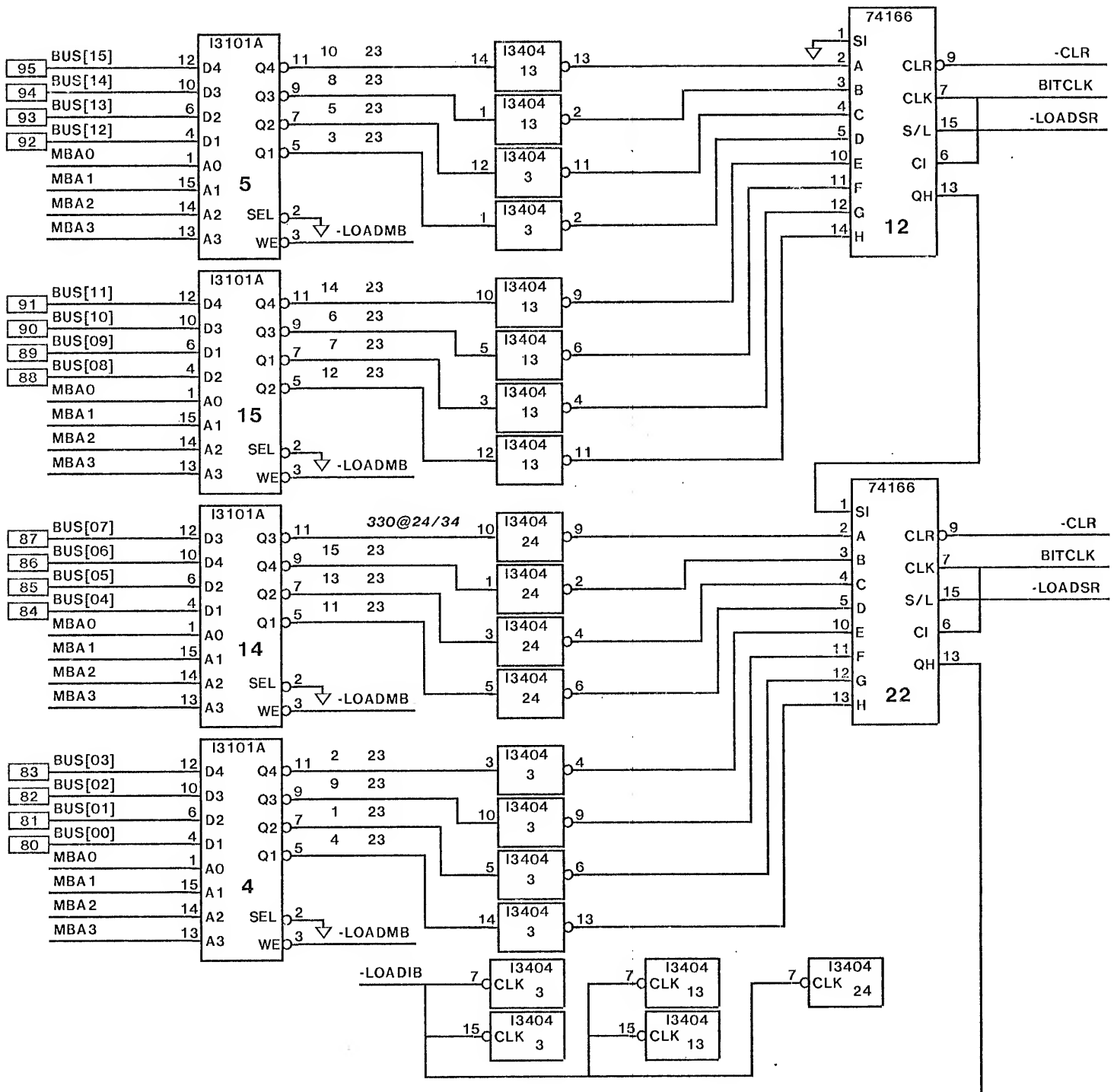


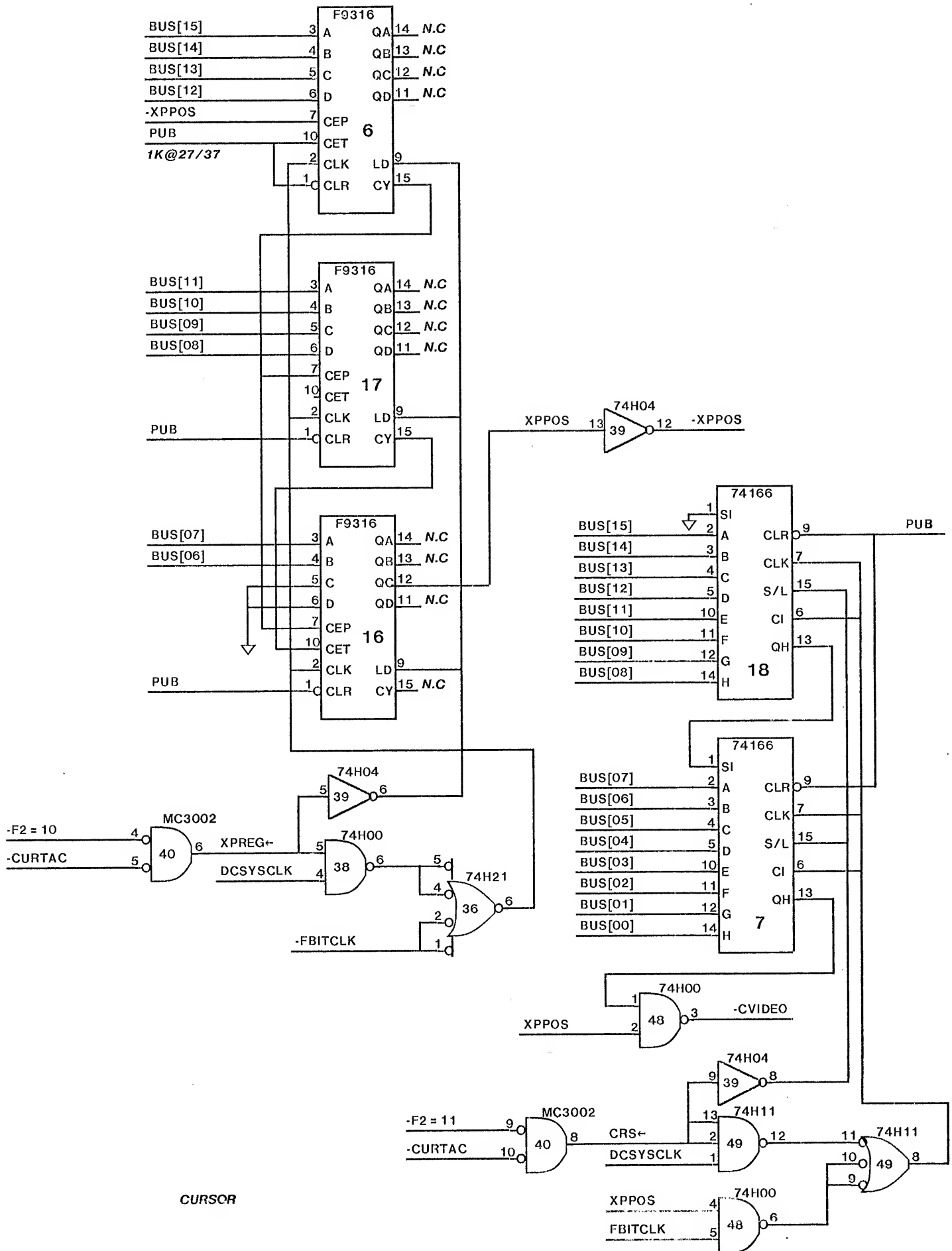


BUFFER CONTROL



VIDEO BIT CLOCK



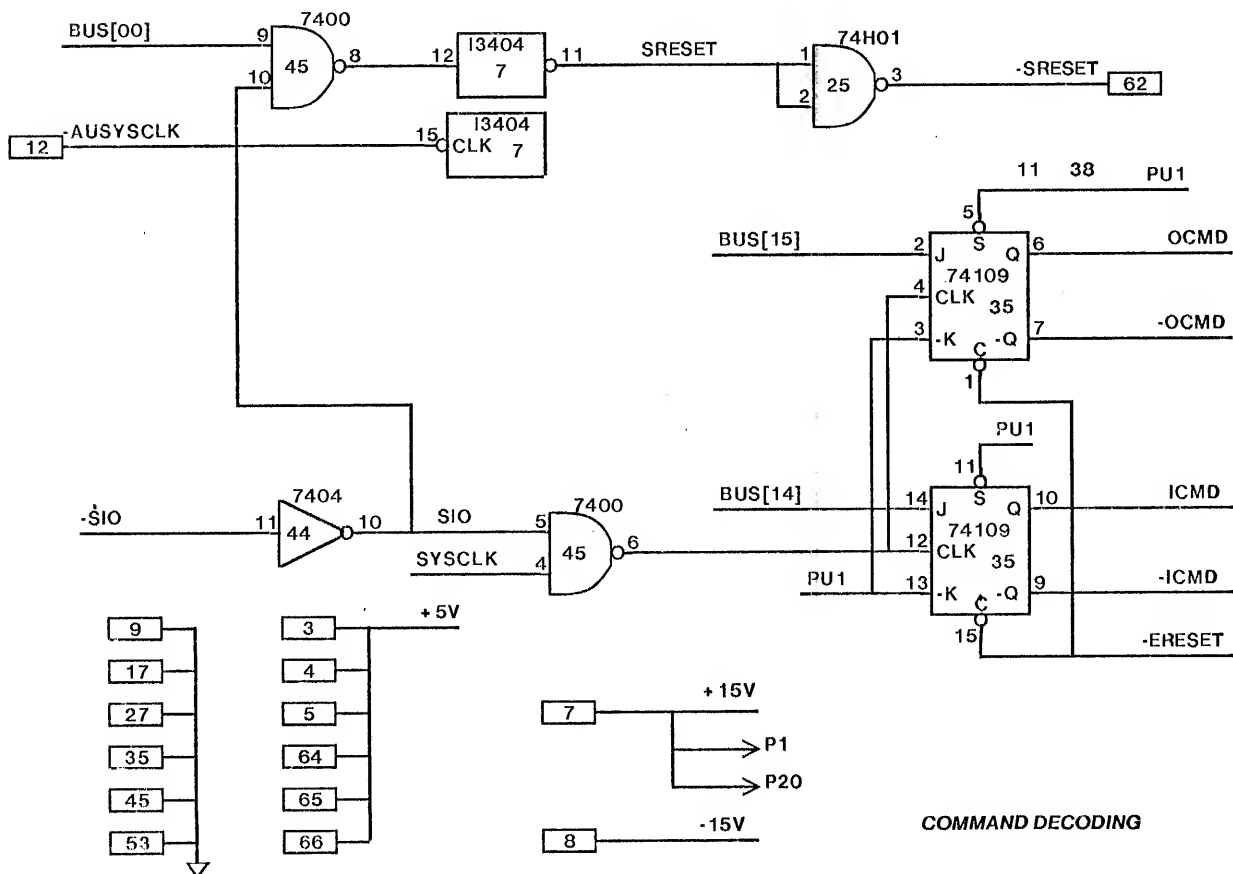
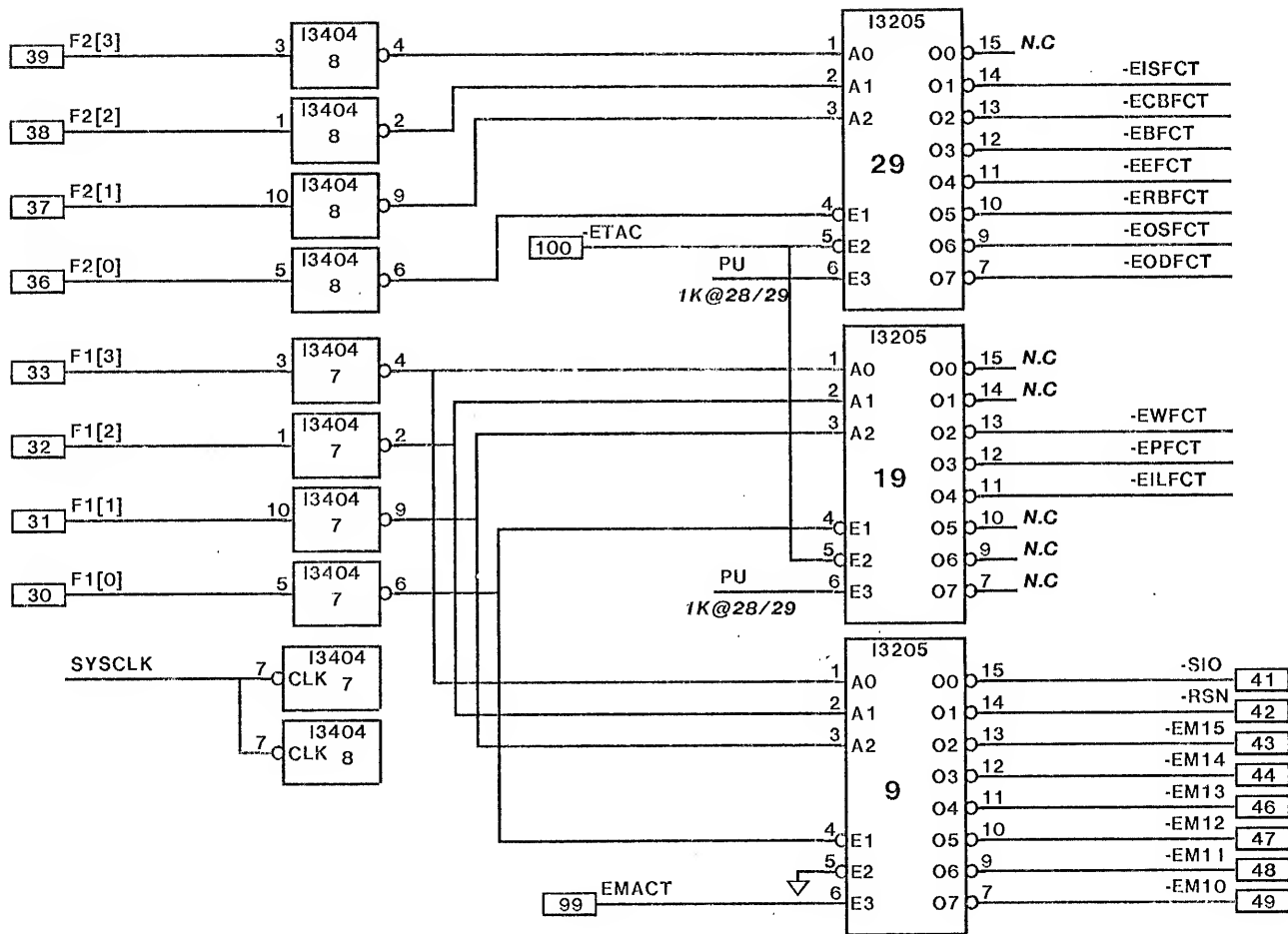


DISPLAY Page 6

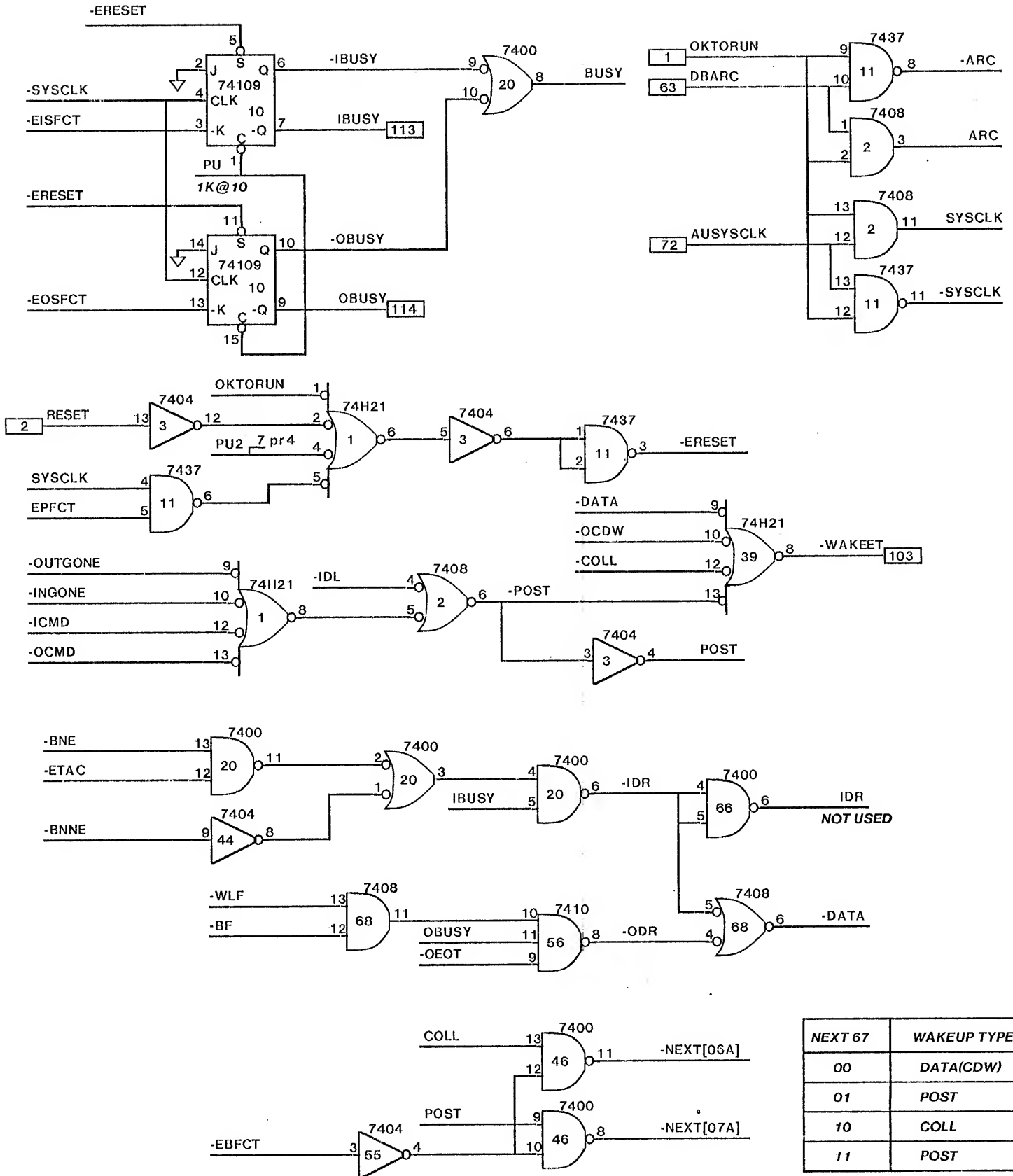


DISPLAY Page 7



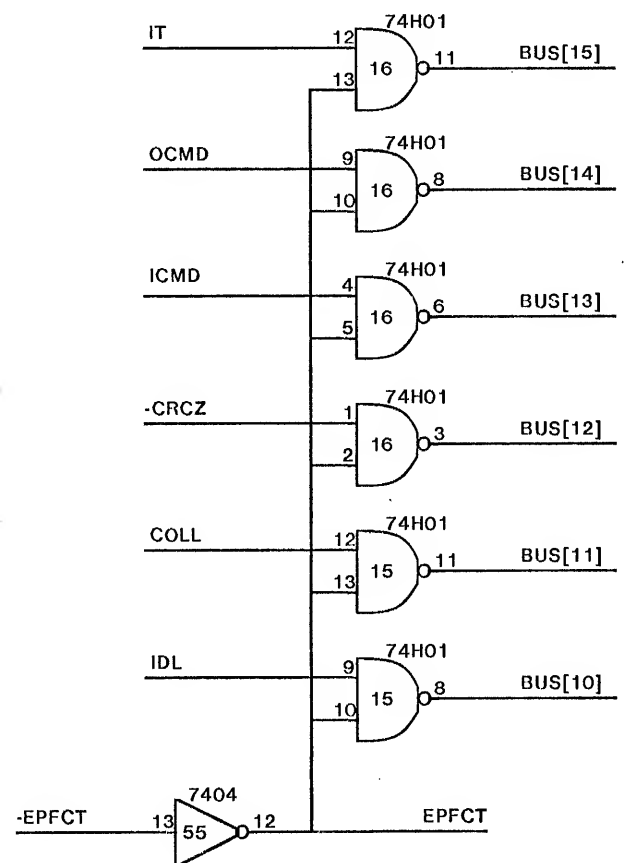
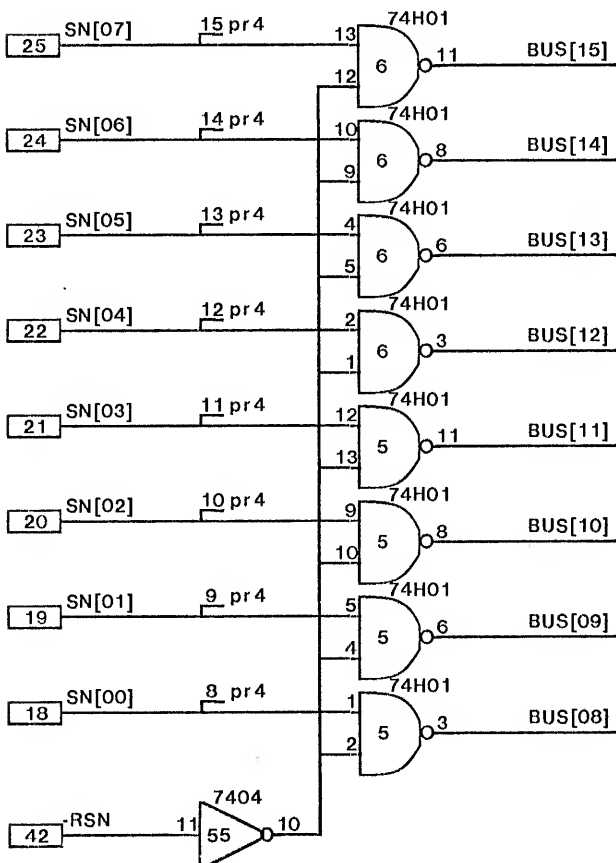
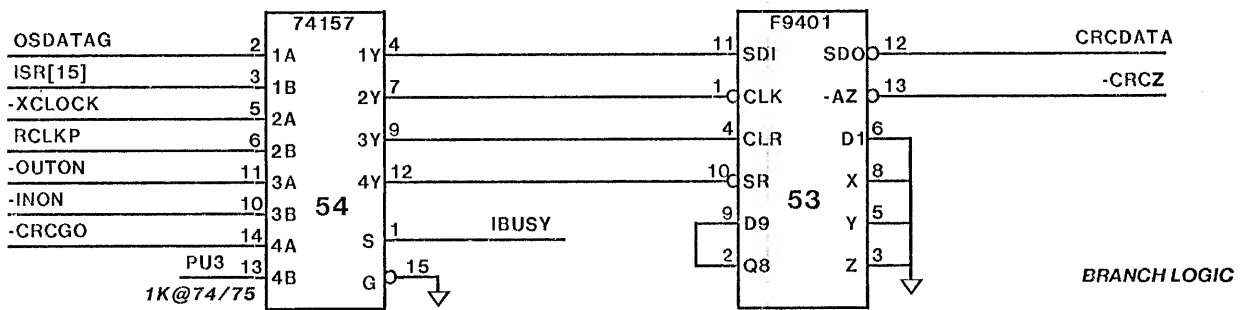
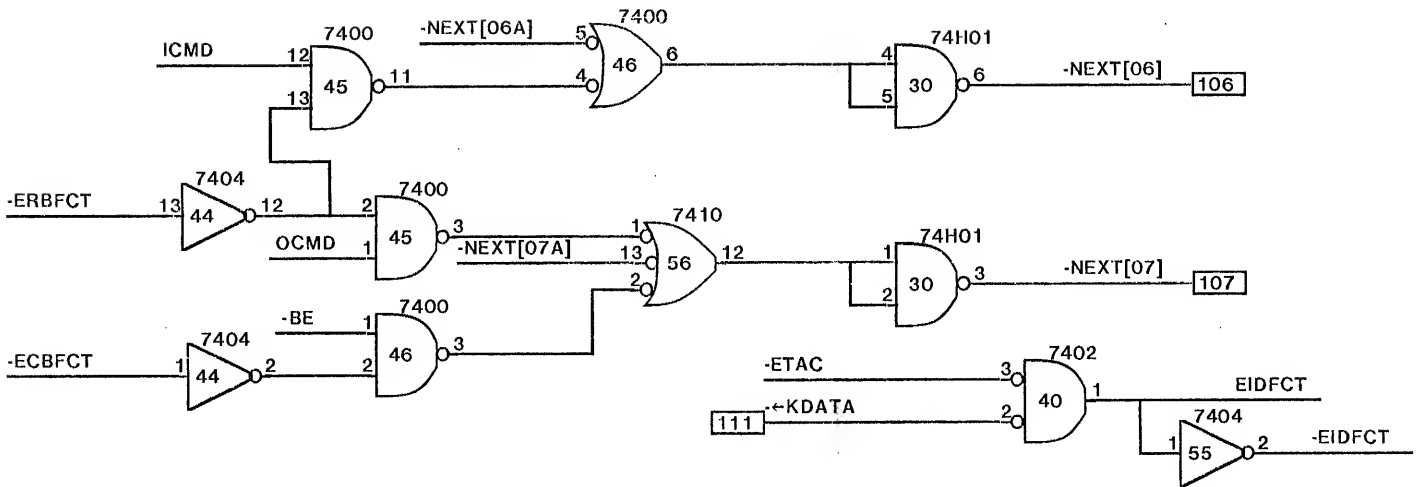


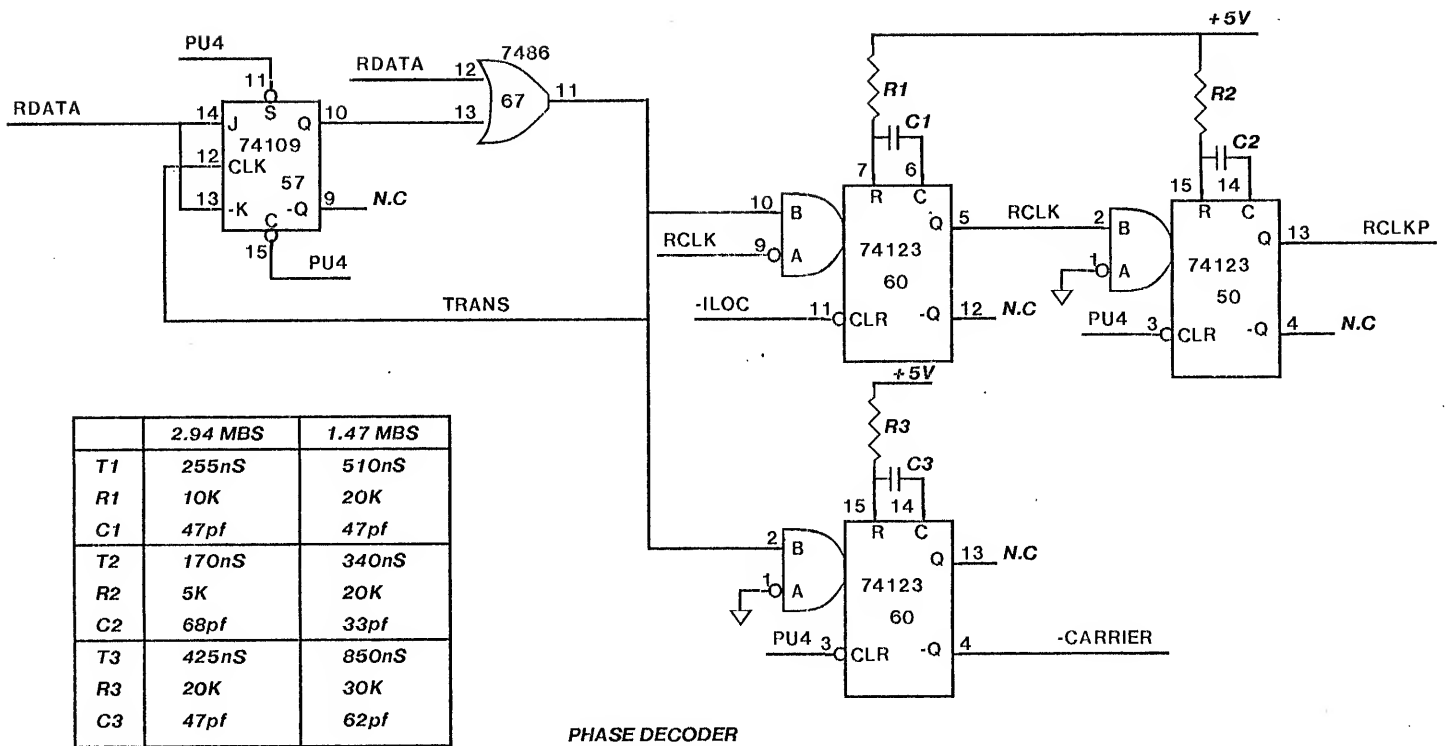
COMMAND DECODING



ALTO INTERFACE

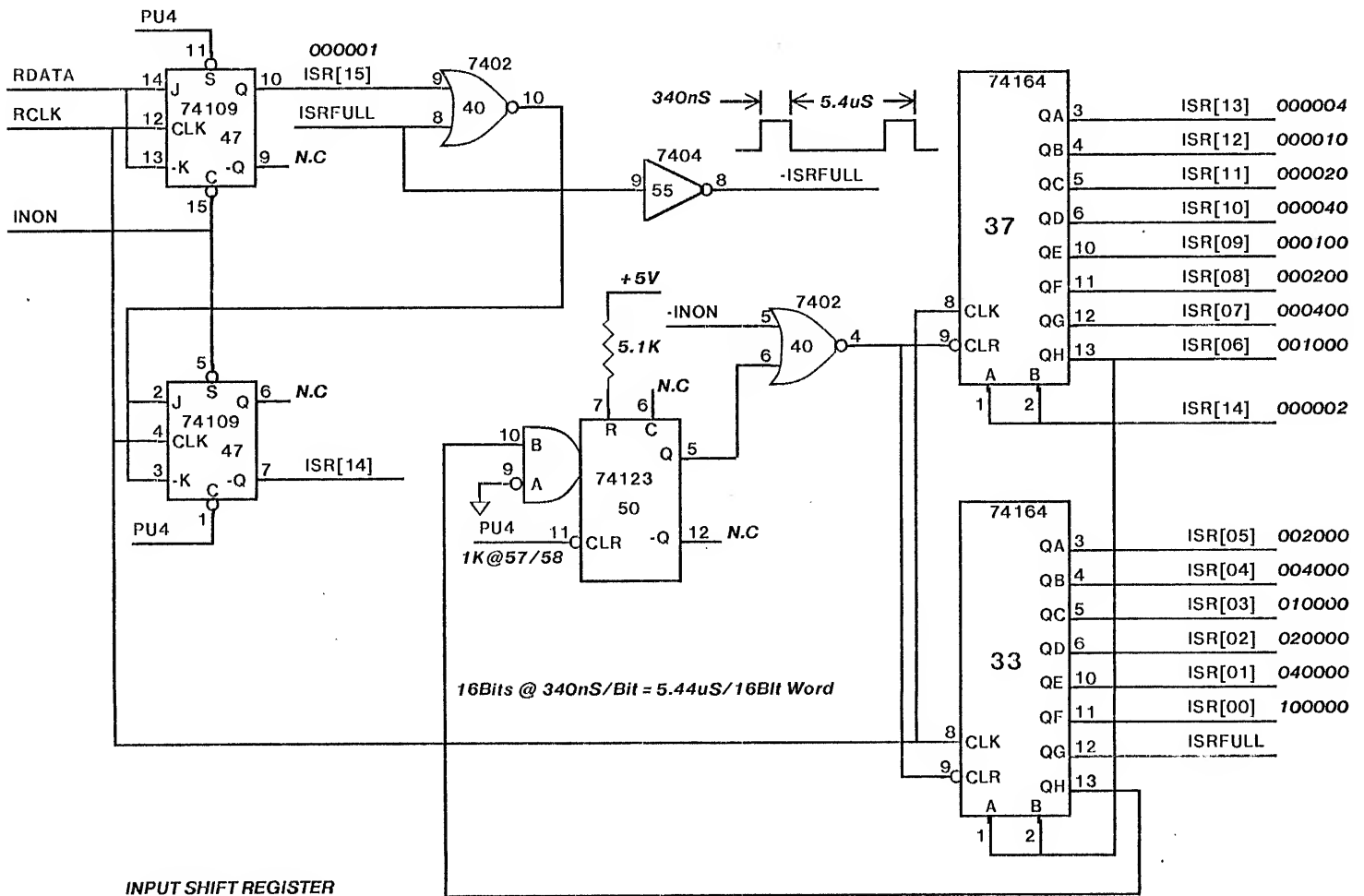


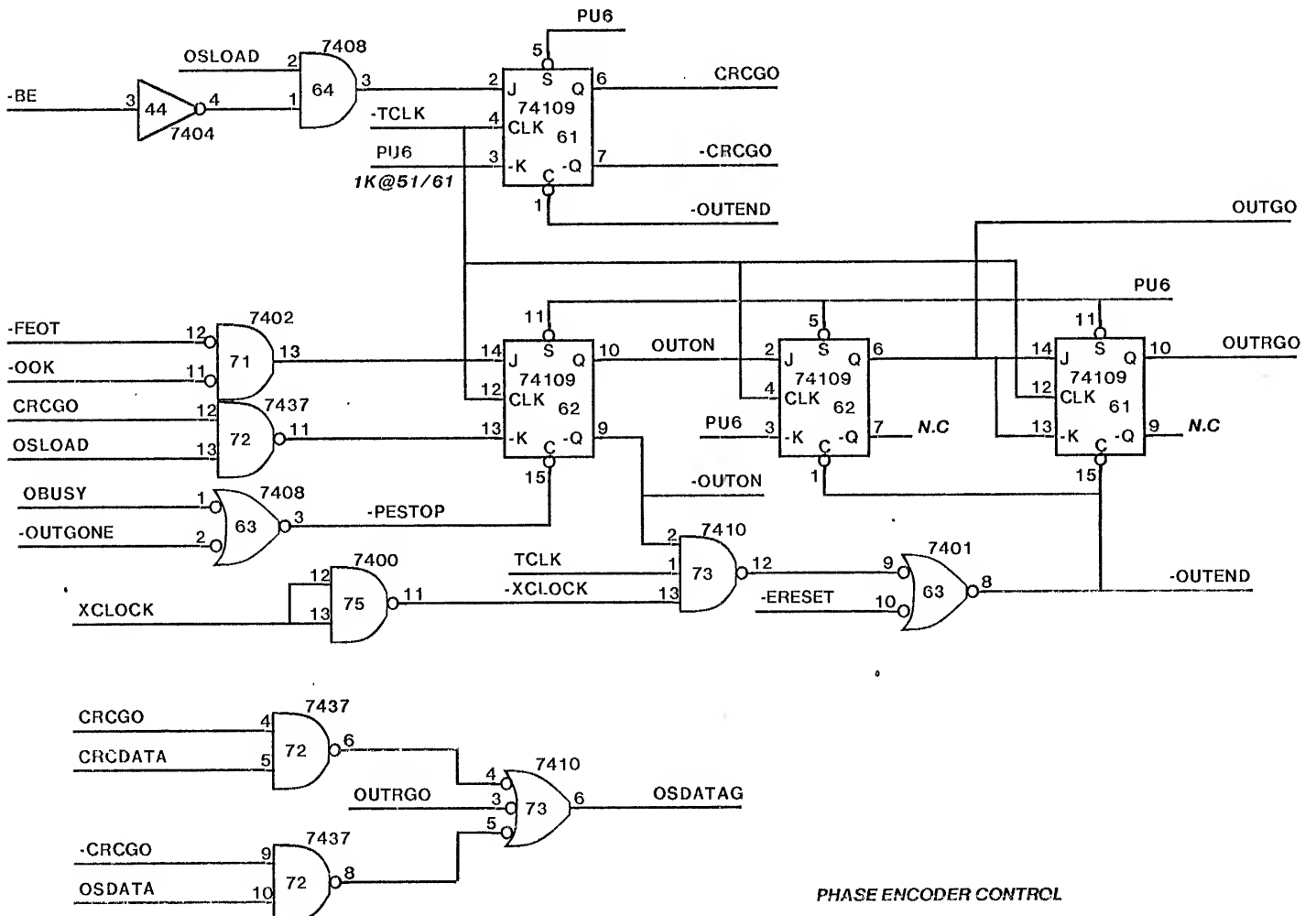
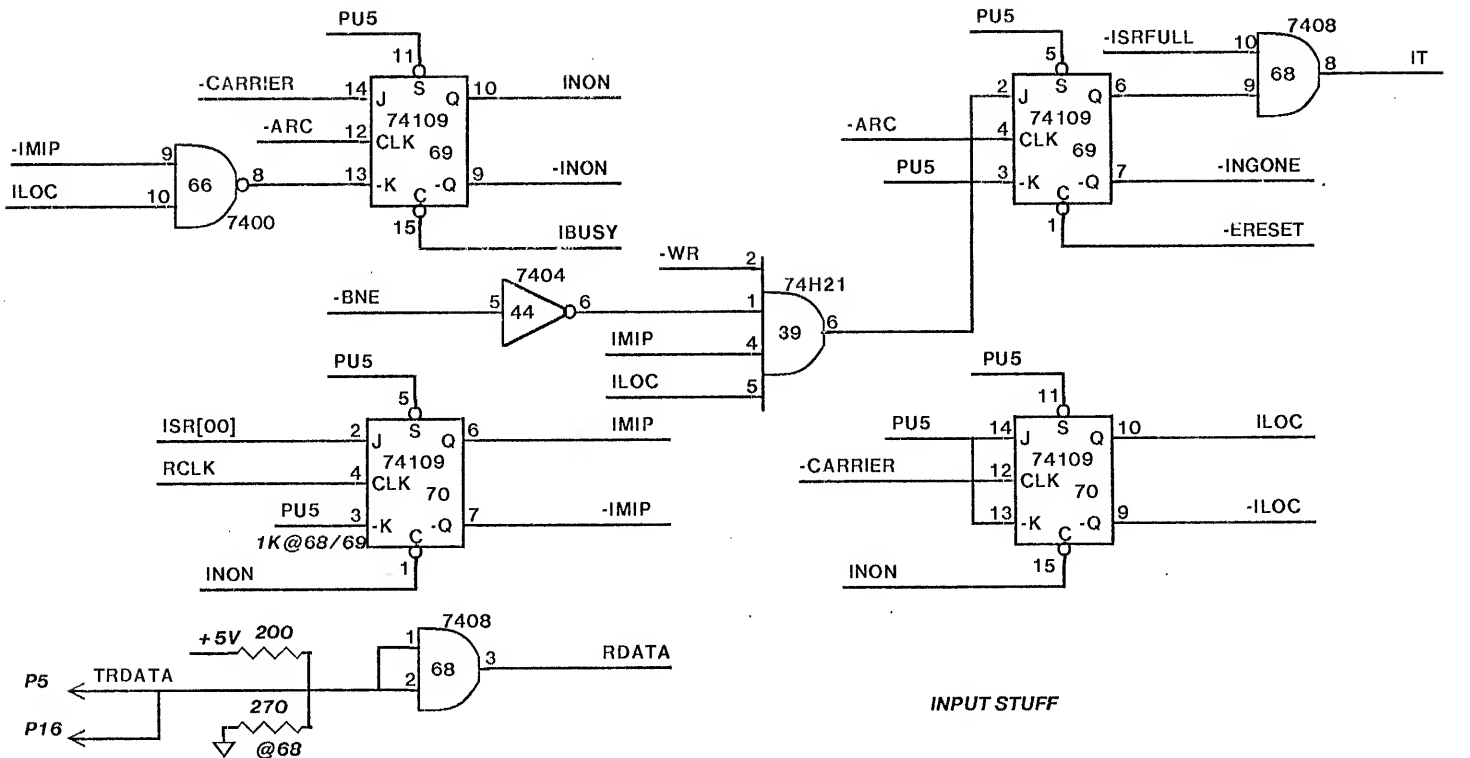


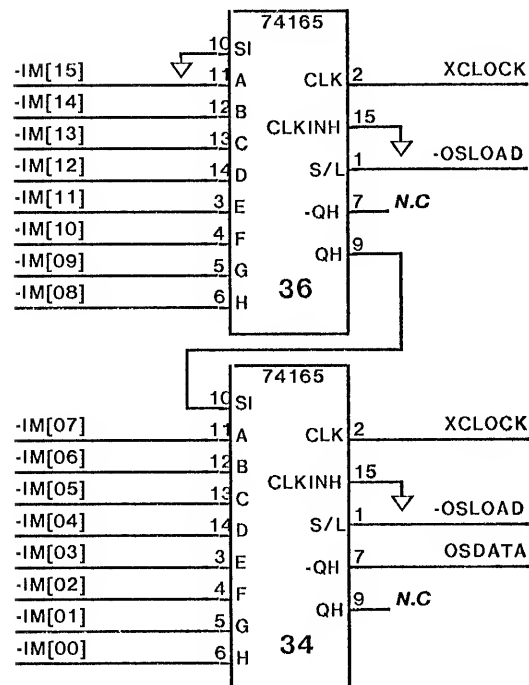
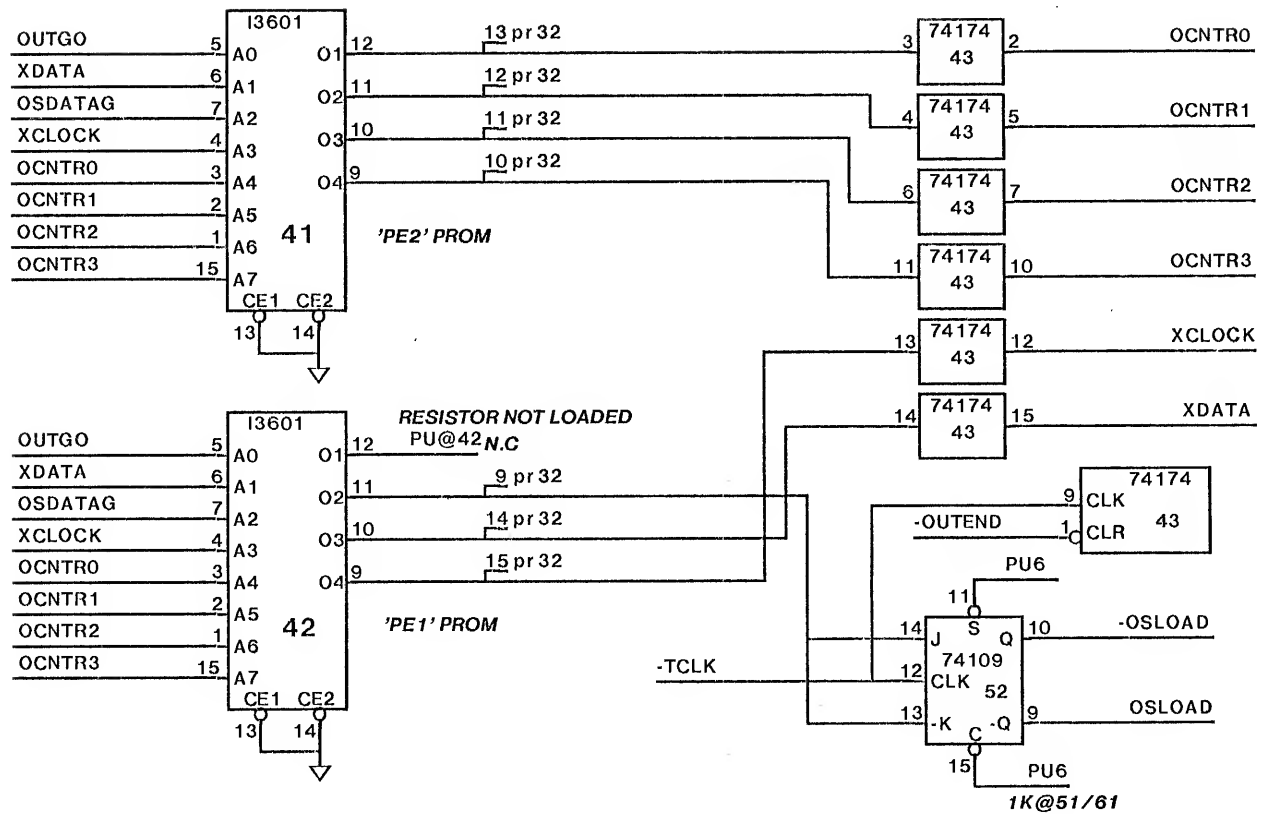


	2.94 MBS	1.47 MBS
T1	255nS	510nS
R1	10K	20K
C1	47pf	47pf
T2	170nS	340nS
R2	5K	20K
C2	68pf	33pf
T3	425nS	850nS
R3	20K	30K
C3	47pf	62pf

## PHASE DECODER

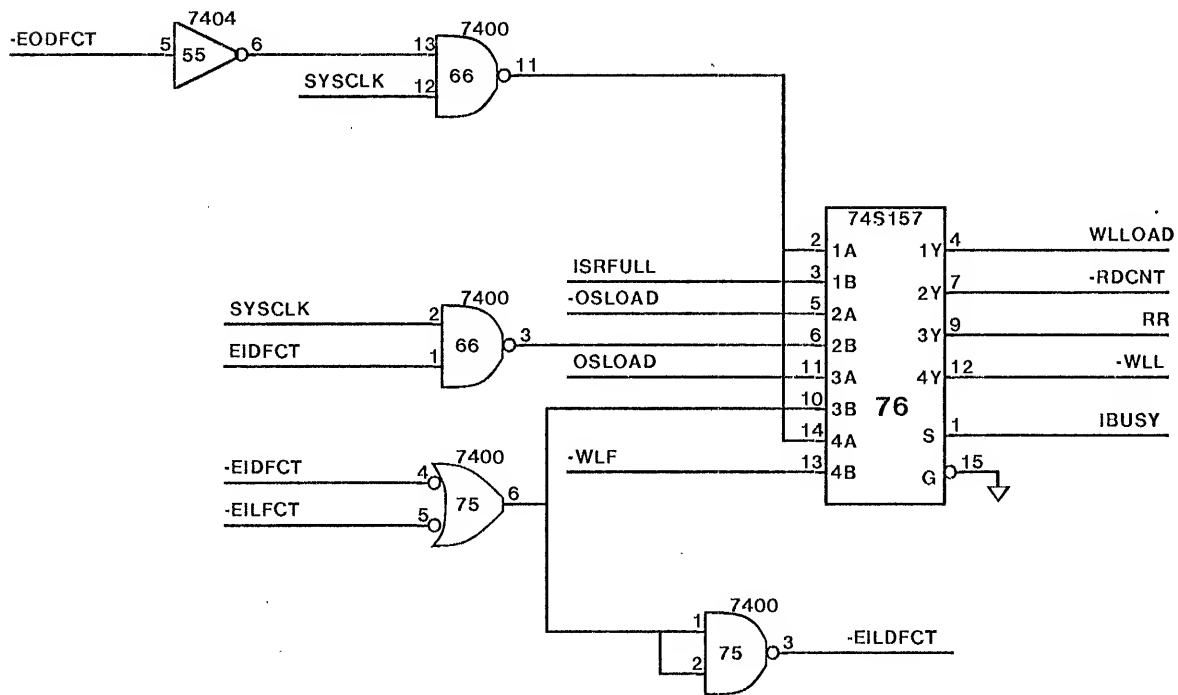




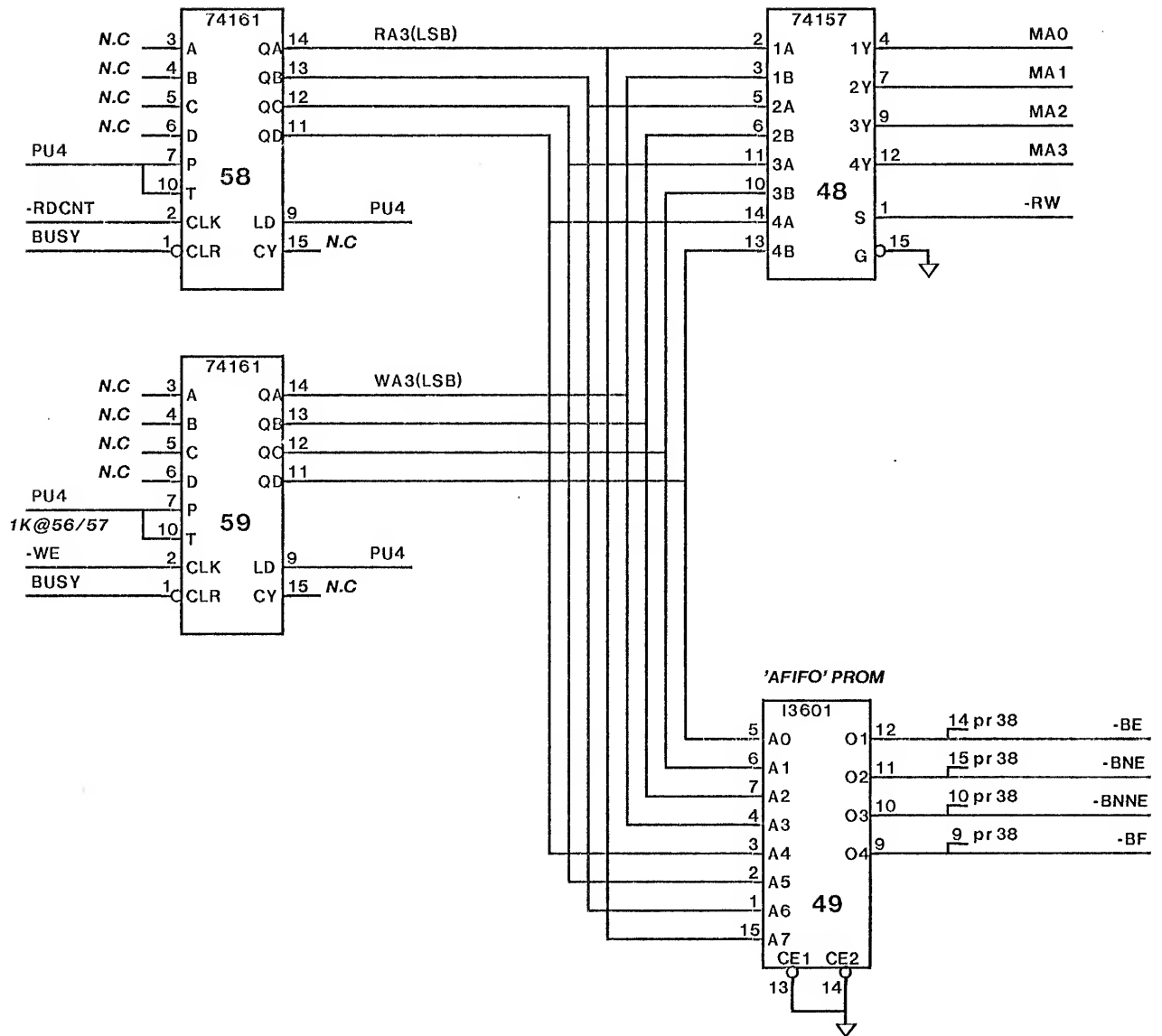


OUTPUT SHIFT REGISTER &amp; ENCODER

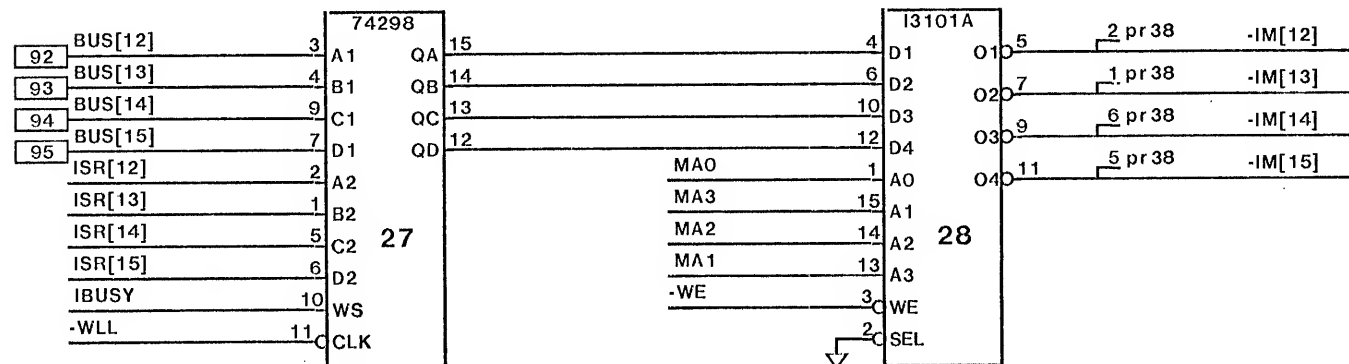
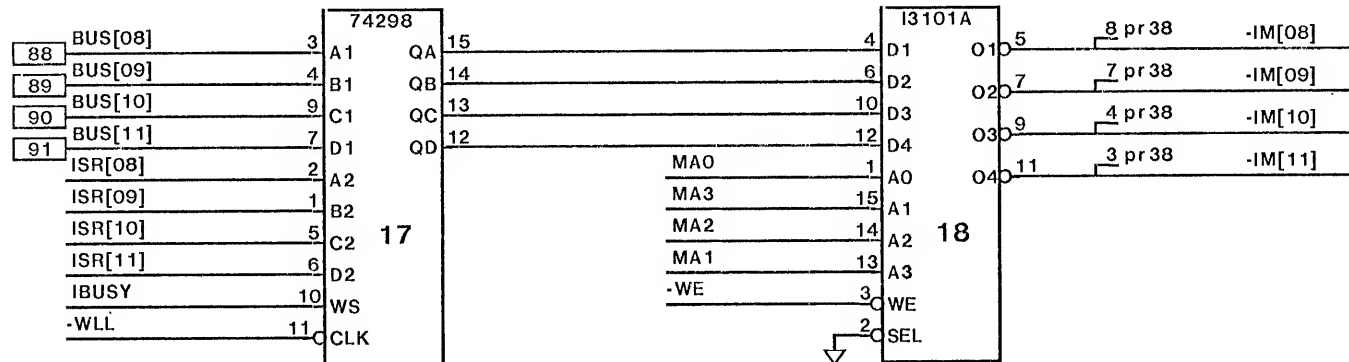
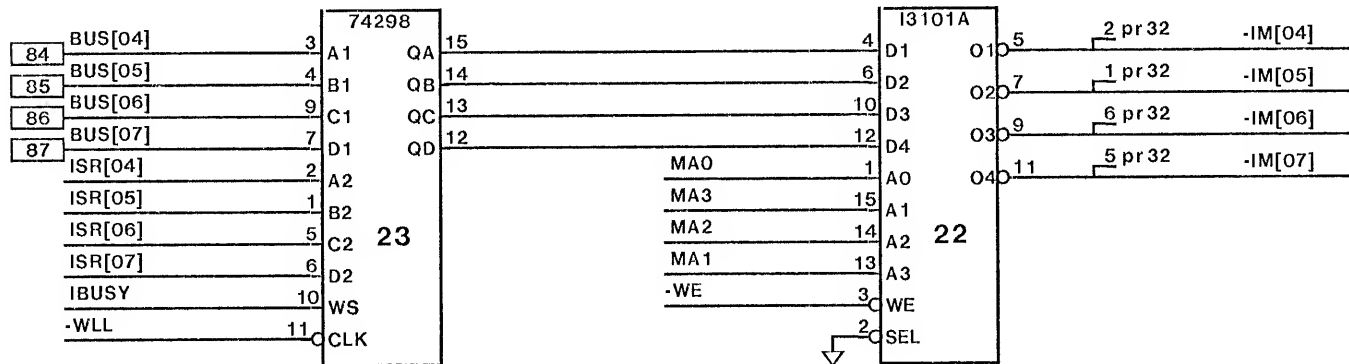
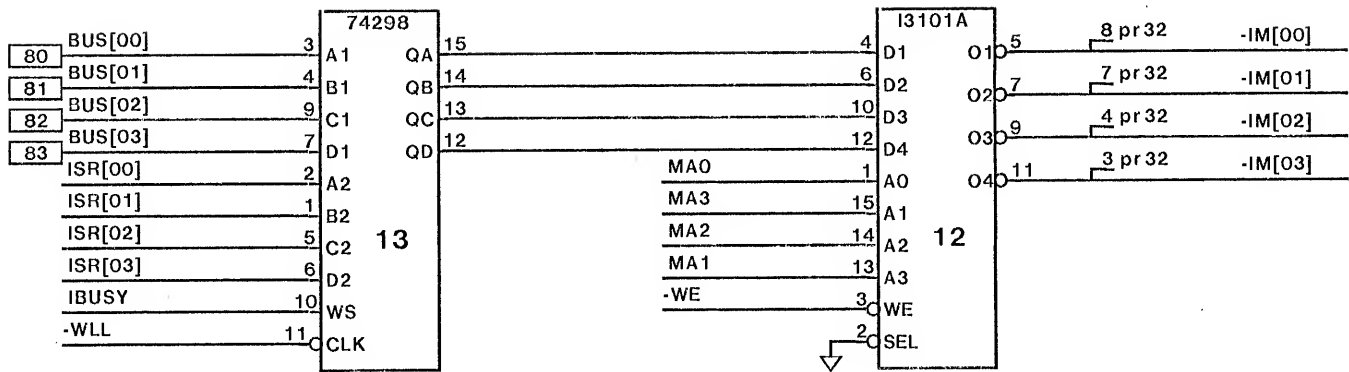
ETHERNET Page 7



### ***BUFFER CONTROL***

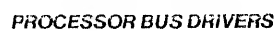


HALF DUPLEX BUFFER



HALF DUPLEX BUFFER

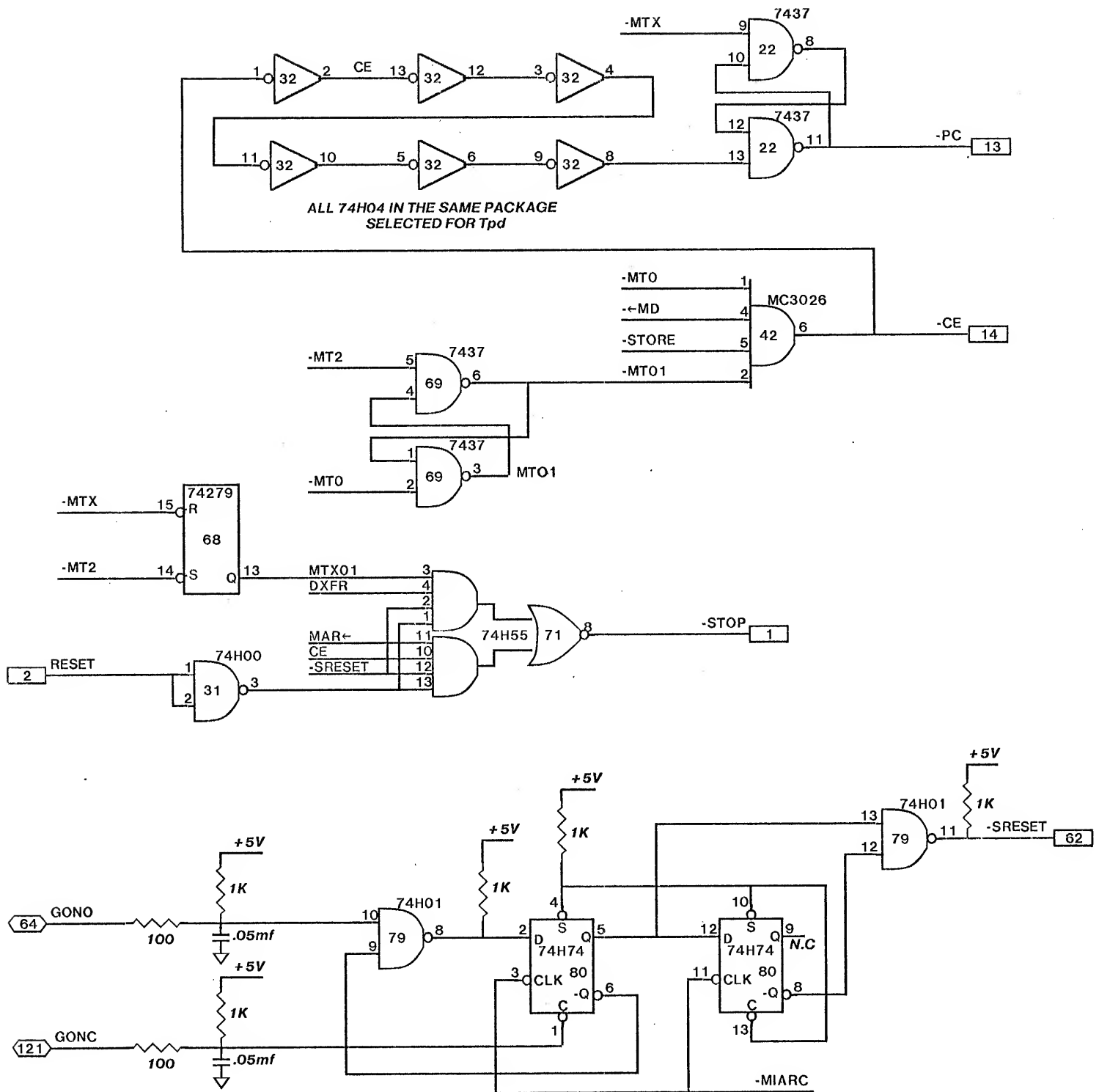
ETHERNET Page 10





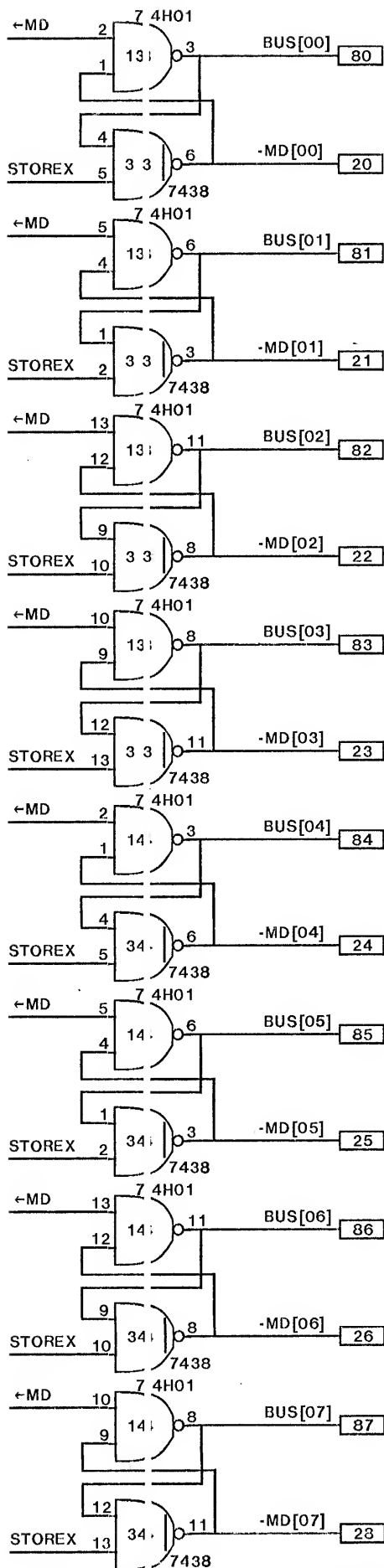
MEMORY INT Page 1





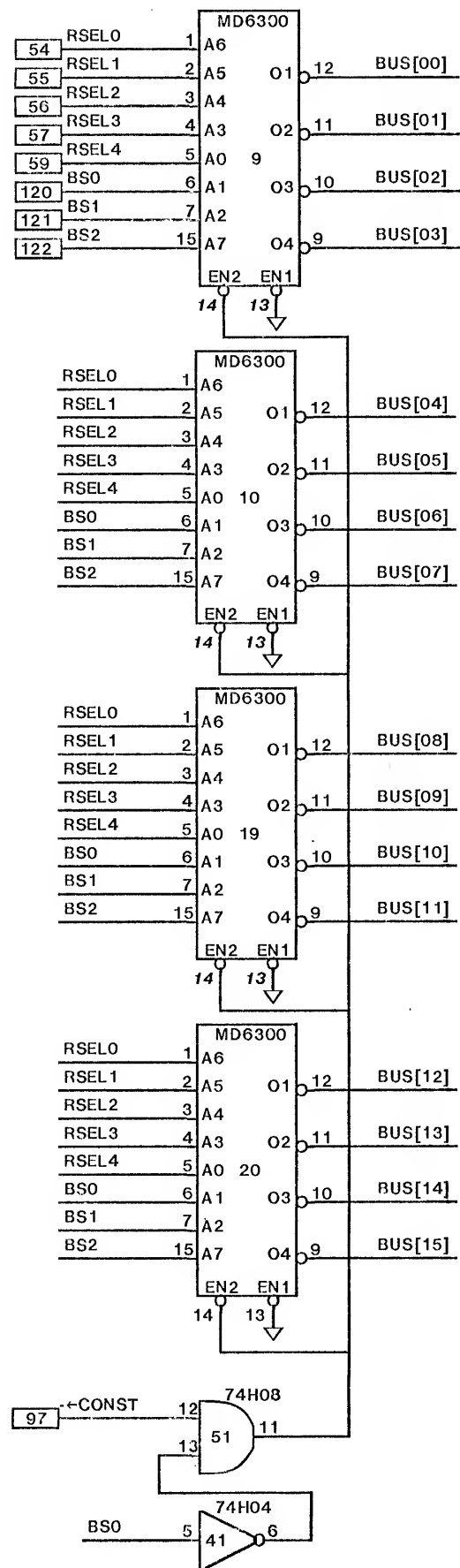
6 JAN 77

MEM INT Page 3

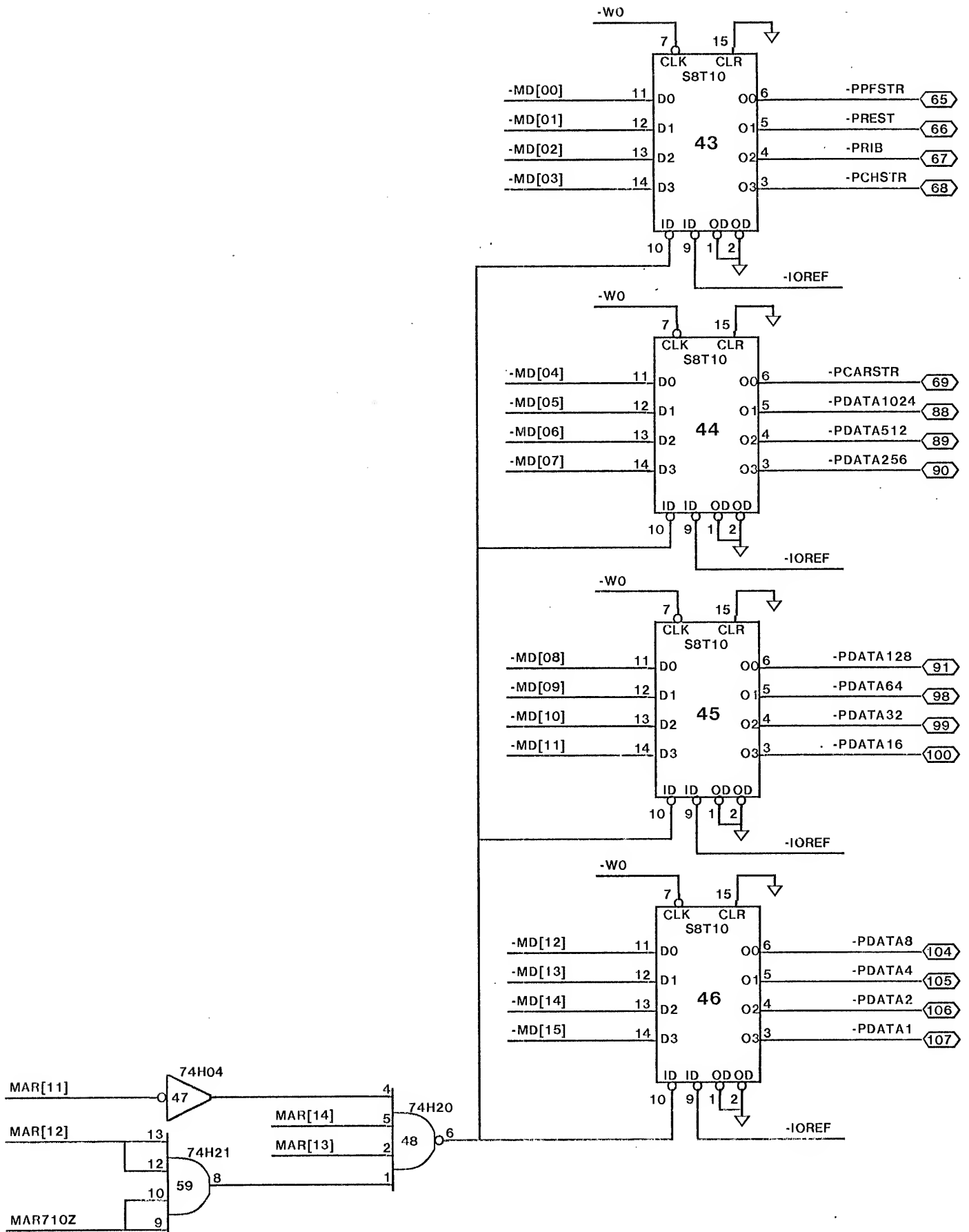


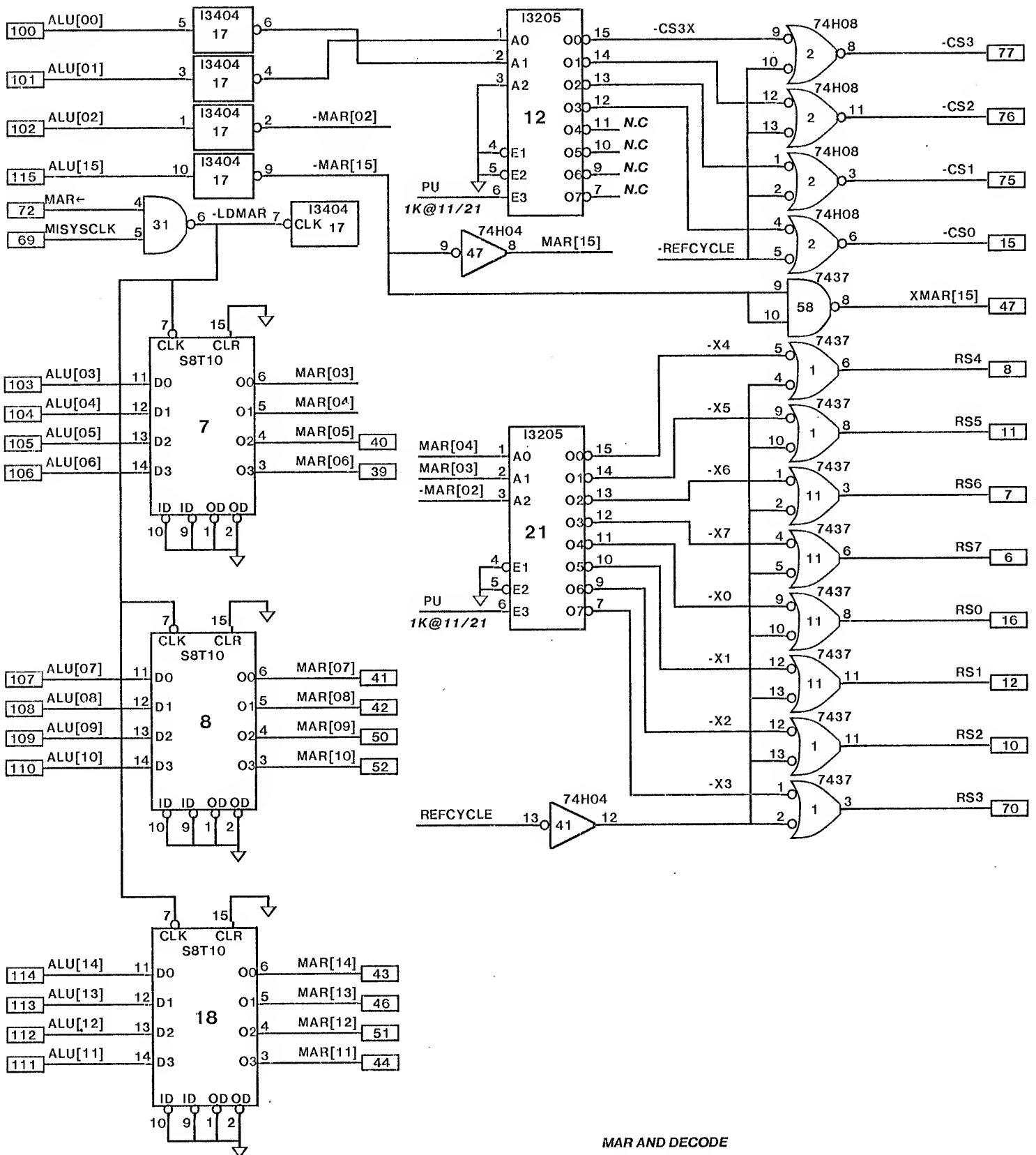
BUS DRIVER'S

ALL -MD SIGNALS ARE PULLED UP WITH  
330 OHM DISCRETE RESISTORS ON THE BOARD

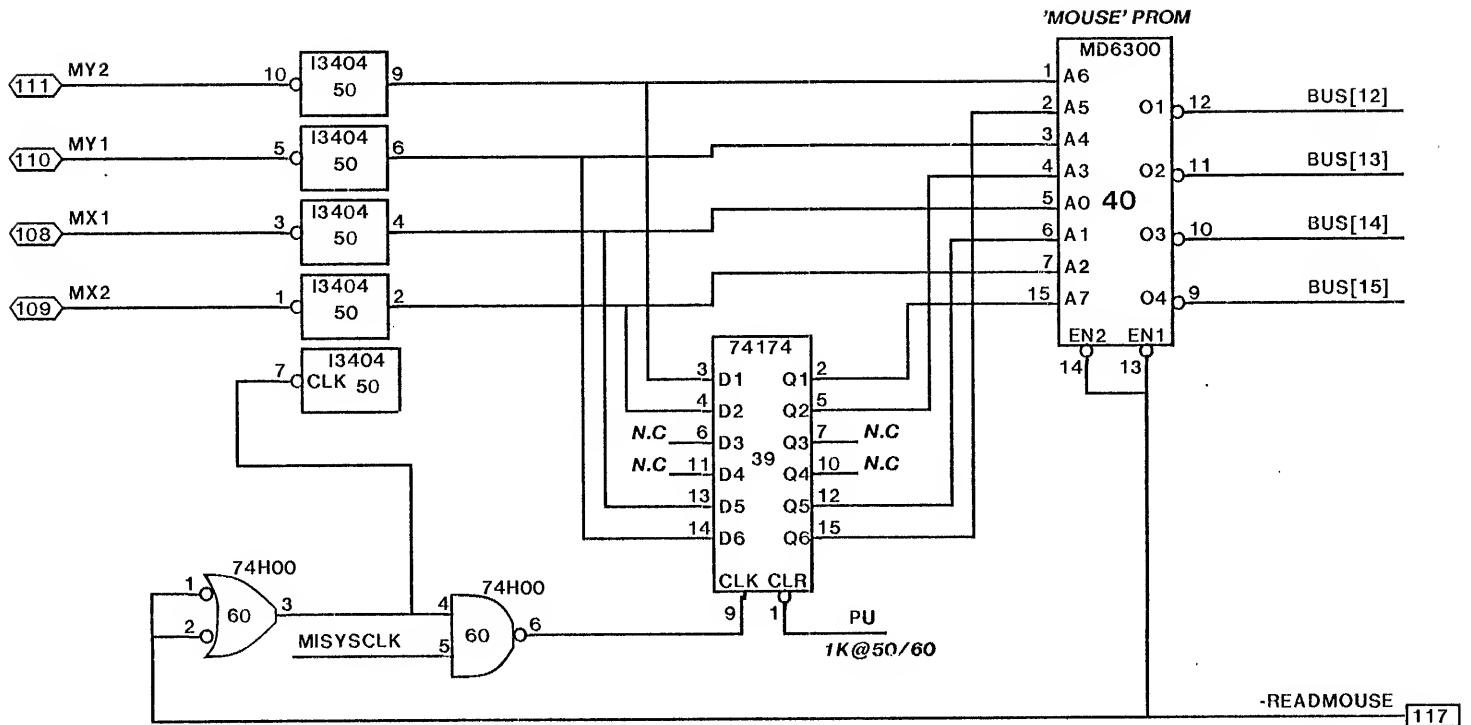
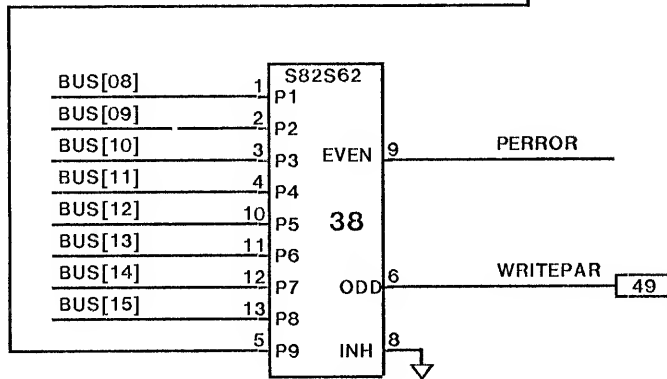
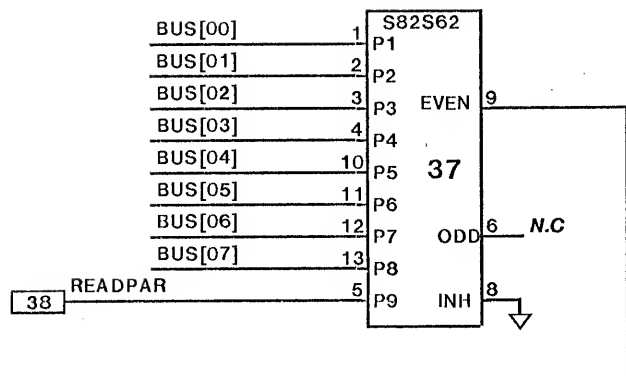


CONSTANT MEMORY'S





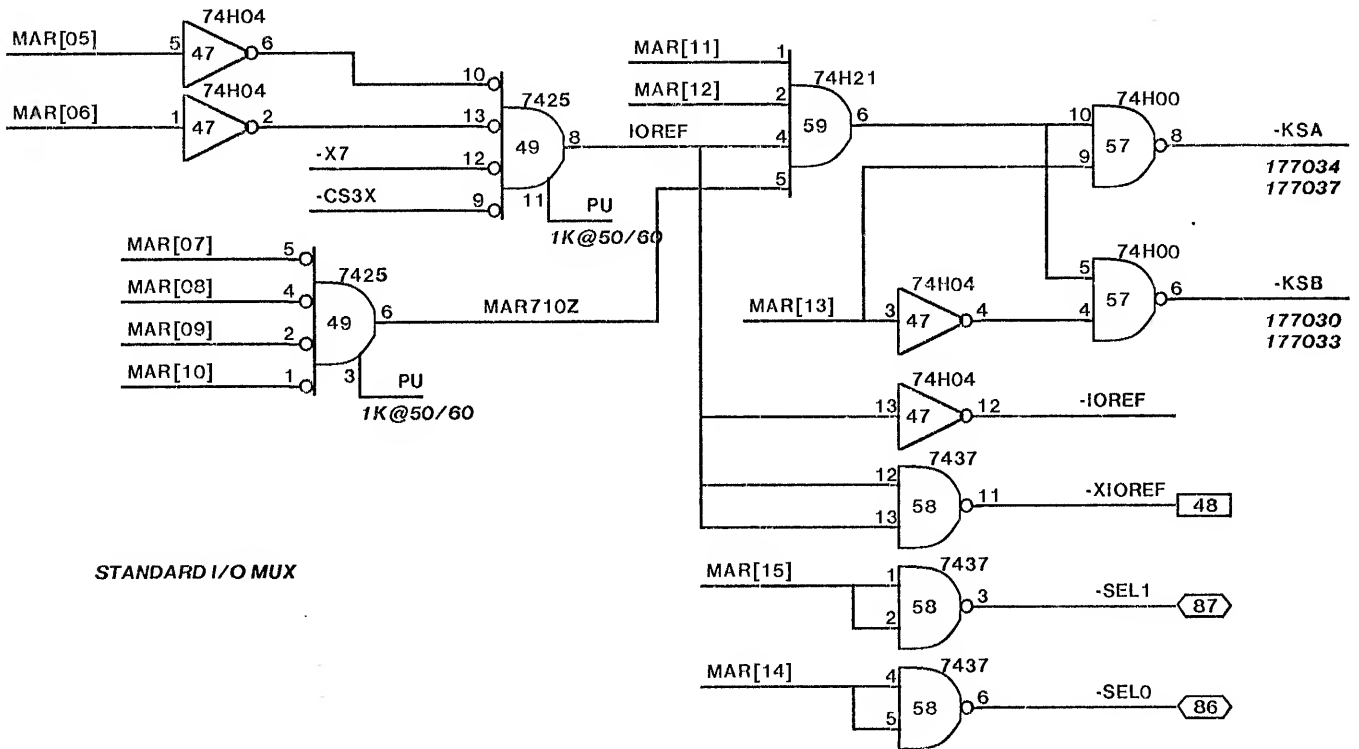
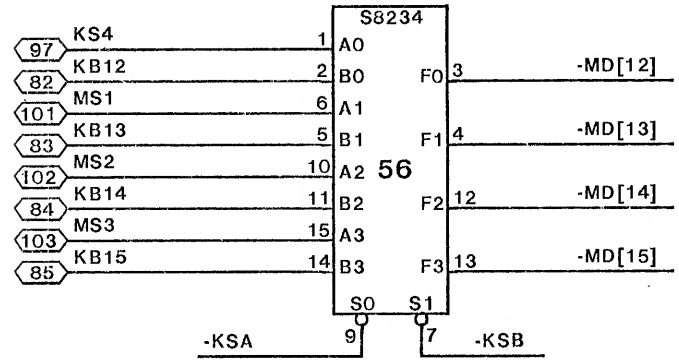
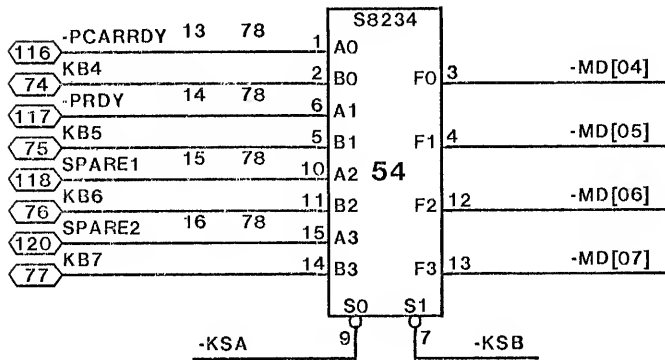
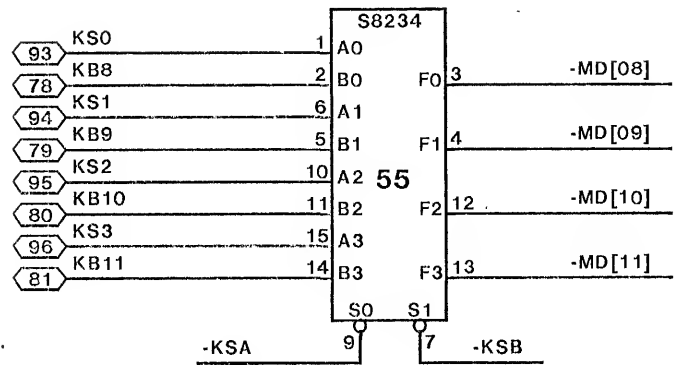
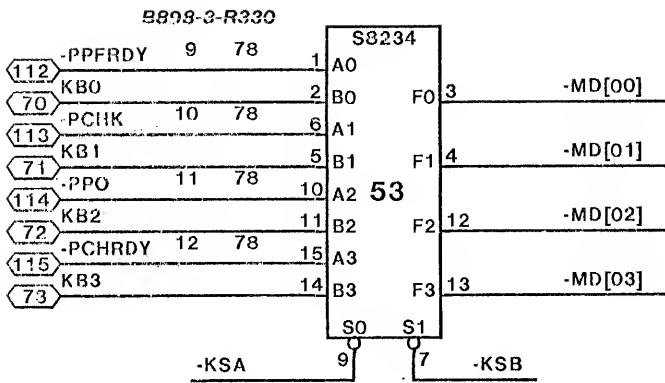
MAR AND DECODE



MOUSE AND PARITY

27 JAN 77

MEMORY INT Page 7



28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory				memory interface	ALU	control	control ram	display controller	disk controller	ethernet		

MEMORY						MEMORY						MEMORY						MEMORY						MEMORY					
1			62			1			62			1			62			1			62			1			62		
2			3			2			3			2			3			2			3			2			3		
3			4			3			4			3			4			3			4			3			4		
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9			100			9			100			9			100			9			100			9			100		
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9			120			9			120			9			120			9			120			9			120		
60			1			60			1			60			1			60			1			60			1		
1			2			1			2			1			2			1			2			1			2		

-5volts  
+5volts

+16volts

+19.5volts



Even  
nos.  
pop.

28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory				memory interface	ALU	control	control ram	display controller	disk controller	ethernet		

← LEFT SIDE

BACKPLANE VIEW FROM FRONT  
OF MACHINE

MEMORY

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	110
50	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

MEMORY

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	110
50	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

MEMORY

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	110
50	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

-5volts

+5volts

+16volts

+19.5volts

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	110
50	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
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4	5
5	6
6	7
7	8
8	9
9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
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8	9
9	110
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3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

1	62
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	70
10	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	80
20	1
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3	4
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6	7
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9	90
30	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	100
40	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	110
50	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	120
60	1
1	2

# BACK PANEL

MEM 11	MOSMEM 10	MEMINT 9	ARITH 8	CONTROL 7	DISPLAY 25	DISK 4
1 0 0 -5V	0 0 -5V	STOP 0 0	0 0	*SRESET 0 0 DBSYSCLK STOP 0 0 DBSYSCLK	0 0	0 0
2 0 0 -5V	0 0 -5V	RESET 0 0	0 0	RESET 0 0 DBARC 0 0 DBARC	RESET 0 0 *SRINC	0 0
3 0 0 +5V	0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V
4 0 0 +5V	0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V
5 0 0 +5V	0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V +5V 0 0 +5V	+5V 0 0 +5V
6 0 0 RS7	0 0 RS7	RS7 0 0 WAKEMRT	0 0	DDR 0 0 WAKEMRT DDR 0 0	*LAT 0 0 *ROCLK	0 0
7 0 0 RS6	0 0 RS6	RS6 0 0 SHAKMRT LOADL 0 0 LOADR	LOADL 0 0 LOADR	LOADL 0 0 LOADR	KSYSCLK 0 0 SHAKMRT KSYSCLK 0 0	*SECT(4)
8 0 0 RS4	0 0 RS4	RS4 0 0 MISYSCLK AUSYSCLK 0 0	LOADT	WAKEST 0 0 LOADT AUSYSCLK 0 0	MISYSCLK WAKEMRT 0 0	*PDATA
9 0 0 RS3	0 0 RS3	GND 0 0 ZS3	GND 0 0	GND 0 0 CSYSCLK	GND 0 0 CSYSCLK	GND 0 0 *DISK
10 0 0 RS2	0 0 RS2	RS2 0 0 MIARC	IR(04) 0 0 IR+	IR(04) 0 0 IR+	0 0 MIARC *ADPACK 0 0	*SRURDY
11 0 0 RS5	0 0 RS5	RS5 0 0 MAR	(41) 0 0 AUSYSCLK	(41) 0 0 MAR	0 0 AUSYSCLK	0 0
12 0 0 RS1	0 0 RS1	RS1 0 0 STORE	(42) 0 0 *CARRY	(42) 0 0 STORE	0 0	0 0
13 0 0 PC	0 0 PC	PC 0 0 SELR37	(43) 0 0 *SKIP	(43) 0 0 SELR37	0 0	0 0
14 0 0 CE	0 0 CE	CE 0 0 CSI	(44) 0 0 DNS	(44) 0 0 DNS	0 0	0 0
15 0 0 CS4	0 0 CS4	CS4 0 0 CS2	(45) 0 0	(45) 0 0 WAKEDVT	0 0 WAKEDVT	0 0
16 0 0 RS6	0 0 RS6	RS6 0 0 CS3	(46) 0 0	IR(46) 0 0 WAKEDHT	0 0 WAKEDHT	*READY 0 0
17 0 0 WI	0 0 WI	GND 0 0 WI	GND 0 0 IR(47)	GND 0 0 IR(47)	GND 0 0	GND 0 0
18 0 0 DS1	0 0 DS1	DS1 0 0 W	(48) 0 0	IR(48) 0 0 WAKEMRT	0 0	*SECT(2) 0 0 WAKEMRT
19 0 0 ML(22)	0 0	DS4 0 0 BUS(44)	(49) 0 0 BUS(44)	IR(49) 0 0 BUS(44)	0 0 BUS(44)	(1) 0 0 BUS(44)
20 0 0 MD(02)	0 0	MD(02) 0 0	(51) 0 0	(51) STOPCLK 0 0	(51) STOPCLK 0 0	(2) 0 0
21 0 0 MD(01)	0 0	(01) 0 0	(02) 0 0	(42) WAKEDVT 0 0	(42) WAKEDVT 0 0	(3) 0 0
22 0 0 MD(03)	0 0	(02) 0 0	(03) 0 0	(43) DVTAC 0 0	(43) DVTAC 0 0	(03) 0 0
23 0 0 MD(01)	0 0	(03) 0 0	(04) 0 0	(44) DHTAC 0 0	(44) DHTAC 0 0	(04) 0 0
24 0 0 MD(04)	0 0	(04) 0 0	(05) 0 0	(45) DWTAC 0 0	(45) DWTAC 0 0	(05) 0 0
25 0 0 MD(02)	0 0	(05) 0 0	(06) 0 0	(46) KWDTAC 0 0	(46) KWDTAC 0 0	(06) 0 0
0 0 MD(03)	0 0	MD(06) 0 0	(07) 0 0	(47) SHZERO 0 0	(47) SHZERO 0 0	(07) 0 0
0 0 MD(04)	0 0	GND 0 0	(08) 0 0	(48) GND 0 0	(48) GND 0 0	(08) 0 0
26 0 0 MD(05)	0 0	MD(07) 0 0	(09) 0 0	(49) KSTAC 0 0	(49) KSTAC 0 0	(09) 0 0
29 0 0 MD(04)	0 0	(08) 0 0	(10) 0 0	(10) 0 0	(10) 0 0	(10) 0 0
30 0 0 MD(05)	0 0	(09) 0 0	(11) 0 0	(11) FI(0) 0 0	(11) FI(0) 0 0	(11) 0 0
31 0 0 MD(07)	0 0	MD(12) 0 0	(12) 0 0	(12) FI(1) 0 0	(12) FI(1) 0 0	(12) 0 0
32 0 0 MD(06)	0 0	(11) 0 0	(13) 0 0	(13) FI(2) 0 0	(13) FI(2) 0 0	(13) 0 0
33 0 0 MD(06)	0 0	(12) 0 0	(14) 0 0	(14) FI(3) 0 0	(14) FI(3) 0 0	(14) 0 0
34 0 0 MD(07)	0 0	MD(13) 0 0	BUS(15) 0 0	ZEROBUS 0 0 BUS(15)	ZEROBUS 0 0 BUS(15)	0 0 BUS(15)
35 0 0 MD(08)	0 0	MD(13) 0 0	GND 0 0	GND 0 0	GND 0 0	GND 0 0
36 0 0 MD(09)	0 0	MD(14) 0 0	CONST+ 0 0	F2(4) 0 0	F2(4) 0 0	F2(4) 0 0
37 0 0 MD(10)	0 0	MD(15) 0 0	F2(1) 0 0	+DISP 0 0	+DISP 0 0	F2(1) 0 0
38 0 0 MD(11)	0 0	READPAR 0 0	F2(2) 0 0	EMACT 0 0	EMACT 0 0	F2(2) 0 0
39 0 0 MAR(02)	0 0	MAR(06) 0 0	ALU(04) 0 0	F2(3) 0 0	NEXT(03) 0 0	F2(3) 0 0
40 0 0 MAR(05)	0 0	MAR(05) 0 0	(31) 0 0	ALUF0 0 0	(31) 0 0	0 0
41 0 0 MAR(07)	0 0	MAR(07) 0 0	(32) 0 0	1 0 0	(32) 0 0	0 0
42 0 0 MAR(08)	0 0	MAR(08) 0 0	(33) 0 0	2 0 0	(33) 0 0	0 0
43 0 0 MAR(14)	0 0	MAR(14) 0 0	(34) 0 0	ALUF3 0 0	(34) 0 0	0 0
44 0 0 MAR(11)	0 0	MAR(11) 0 0	(35) 0 0	BSE0 0 0	(35) 0 0	0 0
45 0 0 MAR(13)	0 0	MAR(13) 0 0	(36) 0 0	GND 0 0	(36) 0 0	0 0
46 0 0 MD(08)	0 0	MD(13) 0 0	(37) 0 0	LSHI 0 0	(37) 0 0	0 0
47 0 0 MD(09)	0 0	MD(14) 0 0	(38) 0 0	RSHI 0 0	(38) 0 0	0 0
48 0 0 MD(10)	0 0	MD(15) 0 0	(39) 0 0	LCYB 0 0	(39) 0 0	0 0
49 0 0 MD(11)	0 0	WRITEPAR 0 0	(40) 0 0	LALUC0 0 0	(40) 0 0	0 0
50 0 0 MAR(09)	0 0	MAR(09) 0 0	(41) 0 0	SH(04) 0 0	(41) 0 0	0 0
51 0 0 MAR(12)	0 0	MAR(12) 0 0	(42) 0 0	F2+10 0 0	(42) 0 0	0 0
52 0 0 MAR(10)	0 0	MAR(10) 0 0	(43) 0 0	0 0	(43) 0 0	0 0
53 0 0 +16V	0 0 +16V	GND 0 0	(14) 0 0	GND 0 0	CURTAC 0 0	GND 0 0
0 0 +16V	0 0 +16V	RSEL 0 0	ALU(15) 0 0	RSEL 0 0	WAKECURT 0 0	*DISK 0 0
0 0 +16V	0 0 +16V	1 0 0	0 0	FZ+11 0 0	0 0	*HEAD 0 0
56 0 0 +16V	0 0 +16V	2 0 0	READMOS 0 0	2 0 0	READMOS 0 0	*CYL(0) 0 0
57 0 0 +20V	0 0 +20V	3 0 0	WAKEPART 0 0	3 0 0	WAKEPART 0 0	*CYL(2) 0 0
58 0 0	0 0	0 0	0 0	0 0	0 0	0 0
59 0 0 +20V	0 0 +20V	RSEL4 0 0	BS4 0 0	RSEL4 0 0	BS4 0 0	*CYL(4) 0 0
60 0 0 +20V	0 0 +20V	0 0	BS1 0 0	0 0	BS1 0 0	*CYL(6) 0 0
61 0 0 +20V	0 0 +20V	PARTAC 0 0	BS2 0 0	PARTAC 0 0	BS2 0 0	*CYL(8) 0 0

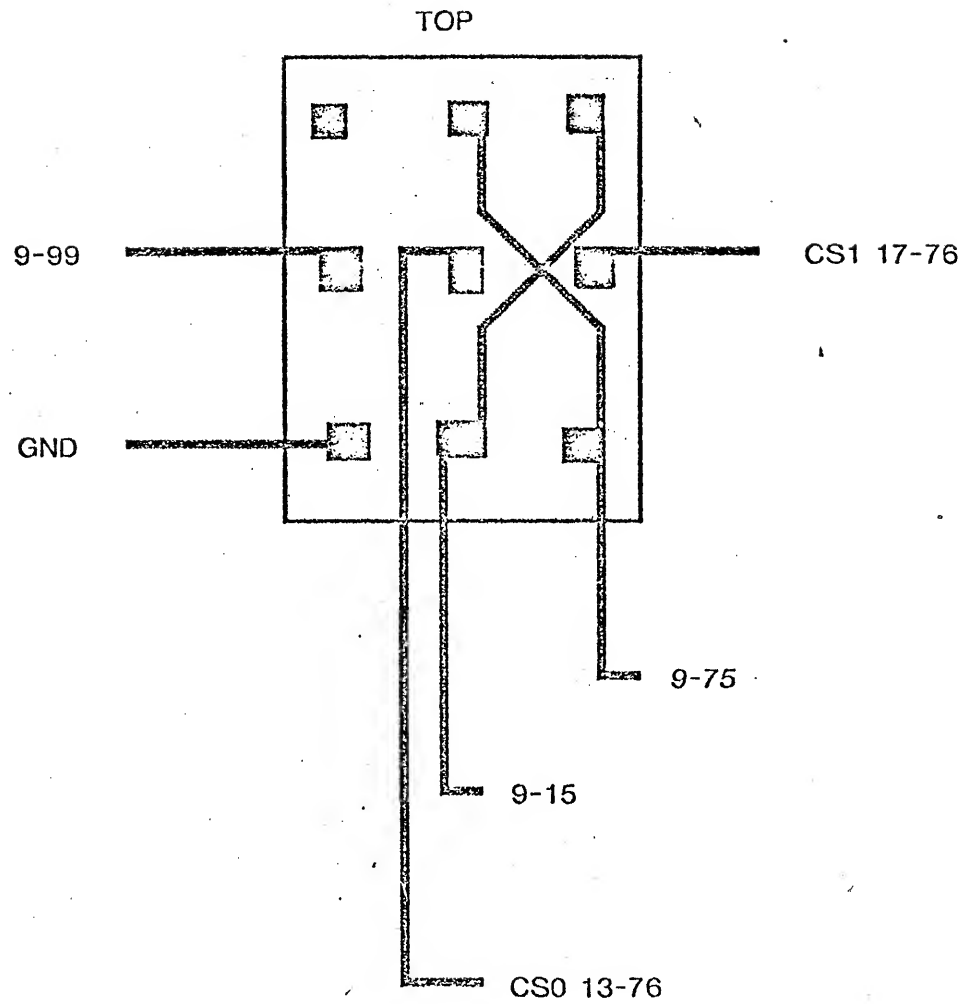
## ALTO MEMORY ARRANGEMENT PRINTED CIRCUIT VERSION

ADDRESS MINIMUM	ADDRESS MAXIMUM	CARD ROW	CARD SLOT
000000	003777	0	EVEN ADDRESSES
004000	007777	1	13 - BITS 0-11
010000	013777	2	14 - BITS 12-15 & PARITY
014000	017777	3	
020000	023777	4	ODD ADDRESSES
024000	027777	5	15 - BITS 0-11
030000	033777	6	16 - BITS 12-15 & PARITY
034000	037777	7	
040000	043777	0	EVEN ADDRESSES
044000	047777	1	17 - BITS 0-11
050000	053777	2	18 - BITS 12-15 & PARITY
054000	057777	3	
060000	063777	4	ODD ADDRESSES
064000	067777	5	19 - BITS 0-11
070000	073777	6	20 - BITS 12-15 & PARITY
074000	077777	7	
100000	103777	0	EVEN ADDRESSES
104000	107777	1	21 - BITS 0-11
110000	113777	2	22 - BITS 12-15 & PARITY
114000	117777	3	
120000	123777	4	ODD ADDRESSES
124000	127777	5	23 - BITS 0-11
130000	133777	6	24 - BITS 12-15 & PARITY
134000	137777	7	
140000	143777	0	EVEN ADDRESSES
144000	147777	1	25 - BITS 0-11
150000	153777	2	26 - BITS 12-15 & PARITY
154000	157777	3	
160000	163777	4	ODD ADDRESSES
164000	167777	5	27 - BITS 0-11
170000	173777	6	28 - BITS 12-15 & PARITY
174000	177777	7	

odd slots

WORD BIT	CARD COLUMN	EVEN SLOTS	WORD BIT	CARD COLUMN
0	0	12	12	7
1	1	13	13	8
2	2	14	14	9
3	3	15	15	10
4	4	PAR	PAR	11
5	5			
6	6			
7	7			
8	8			
9	9			
10	10			
11	11			

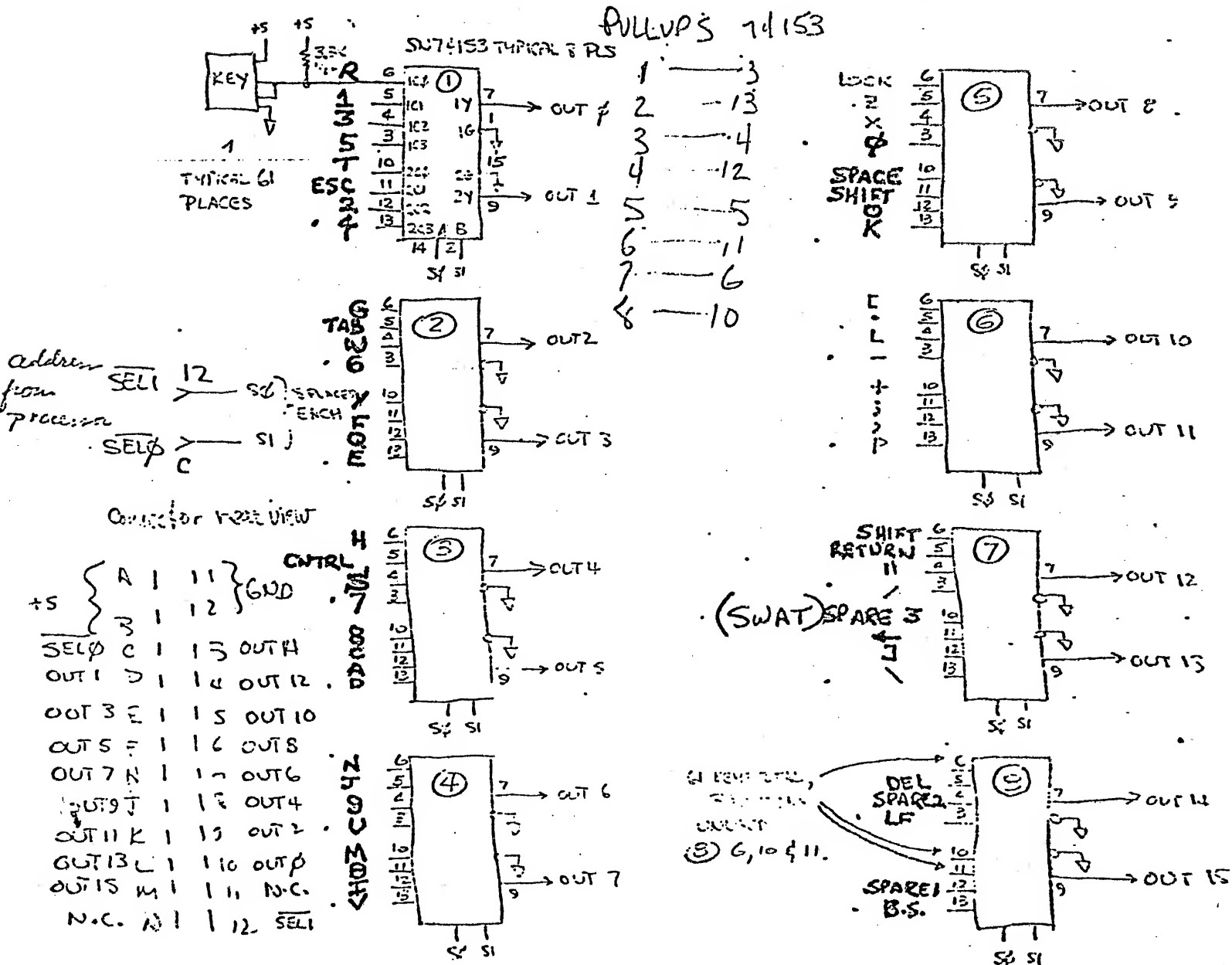
## ALTO MEMORY SWITCH



12-18 Output S/D high when key depressed

### KEYBOARD:

The keyboard has 61 keys. It will receive a 2 bit address from the processor which will select one of four groups of key signals to be gated to the 16 output lines. Output lines are low when key is depressed. The keyboard requires an 18 line (plus power) interface to the processor; 16 data lines and two address lines. The four groups include 16, 16, 16, 13 keys respectively. The relation between keys and bits in the output word is not important, and will be determined primarily by PC layout considerations.



SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
GONO	A/ 1	#26	BUTTON NORMALLY OPEN CONTACT	BLUE/BLACK
KBO	2		D/ 10	VIOLET
KB1	3		D/ D	YELLOW/BLACK
KB2	4		D/ 9	BLUE
KB3	5		D/ E	YELLOW/BROWN
KB4	6		D/ 8	GREEN
KB5	7		D/ F	YELLOW/RED
KB6	8		D/ 7	YELLOW
KB7	9		D/ H	YELLOW/ORANGE
KB8	10		D/ 6	ORANGE
KB9	11		D/ J	YELLOW/GREEN
KB10	12		D/ 5	RED
KB11	13		D/ K	YELLOW/BLUE
KB12	14		D/ 4	BROWN
KB13	15		D/ L	YELLOW/VIOLET
KB14	16		D/ 3	BLACK
KB15	17		D/ M	YELLOW/GREY
SEL0'	18		D/ C	WHITE
SEL1'	19		D/ 12	GREY
KS0	20		C/ 11	ORANGE/BLACK
KS1	21		C/ 10	ORANGE/BROWN
KS2	22		C/ 9	ORANGE/RED
KS3	23		C/ 8	ORANGE/BLUE
KS4	24		C/ 7	ORANGE/VIOLET
MS1	25		B/ 14	WHITE/BLACK
MS2	26		B/ 16	WHITE/BROWN
MS3	27		B/ 15	WHITE/RED
MX1	28		B/ 2	WHITE/ORANGE
MX2	29		B/ 1	WHITE/YELLOW
MY1	30		B/ 3	WHITE/GREEN
MY2	31	✓	B/ 4	WHITE/BLUE

PG 3 CF 3

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN
GONO	A/ 64	#24	B/ 1
P.PFSTR <sup>1</sup>	65		C/ 1
PREST <sup>1</sup>	66		C/ 2
PRIB <sup>1</sup>	67		C/ 3
PCHSTR <sup>1</sup>	68		C/ 4
PCARSTR <sup>1</sup>	69		C/ 5
KB0	70		B/ 2
KB1	71		B/ 3
KB2	72		B/ 4
KB3	73		B/ 5
KB4	74		B/ 6
KB5	75		B/ 7
KB6	76		B/ 8
KB7	77		B/ 9
KB8	78		B/ 10
KB9	79		B/ 11
KB10	80		B/ 12
KB11	81		B/ 13
KB12	82		B/ 14
KB13	83		B/ 15
KB14	84		B/ 16
KB15	85		B/ 17
SEL0 <sup>1</sup>	86		B/ 18
SEL1 <sup>1</sup>	87		B/ 19
PDATA1024 <sup>1</sup>	88		C/ 6
PDATA512 <sup>1</sup>	89		C/ 7
PDATA256 <sup>1</sup>	90		C/ 8
PDATA128 <sup>1</sup>	91		C/ 9
KS0	93		B/ 20
KS1	94		B/ 21
KS2	95		B/ 22



## KEYBOARD / PRINTER INTERNAL CABLE

3

4

2/14/74

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN
KS3	A/ 96	#24	B/ 23
KS4	97		B/ 24
PDATA4 <sup>1</sup>	98		C/ 10
PDATA32 <sup>1</sup>	99		C/ 11
PDATA16 <sup>1</sup>	100		C/ 12
MS1	101		B/ 25
MS2	102		B/ 26
MS3	103		B/ 27
PDATA8 <sup>1</sup>	104		C/ 13
PDATA4 <sup>1</sup>	105		C/ 14
PDATA2 <sup>1</sup>	106		C/ 15
PDATA1 <sup>1</sup>	107		C/ 16
MX1	108		B/ 28
MX2	109		B/ 29
MY1	110		B/ 30
MY2	111		B/ 31
PPFRDY <sup>1</sup>	112		C/ 17
PCHK <sup>1</sup>	113		C/ 20
PFO <sup>1</sup>	114		C/ 21
PCHRDY <sup>1</sup>	115		C/ 22
PCARRDY <sup>1</sup>	116		C/ 23
PRDY <sup>1</sup>	117		C/ 24
SPARE1	<del>118</del> 120		B/ 33
SPARE2	<del>120</del> 122		B/ 34
GONC	121		B/ 32
PRINTER LOGIC GROUND	56		C/ 25
" " "	57		C/ 26
" " "	59		C/ 27
" " "	60		C/ 28
" " "	61	V	C/ 29



ALTO

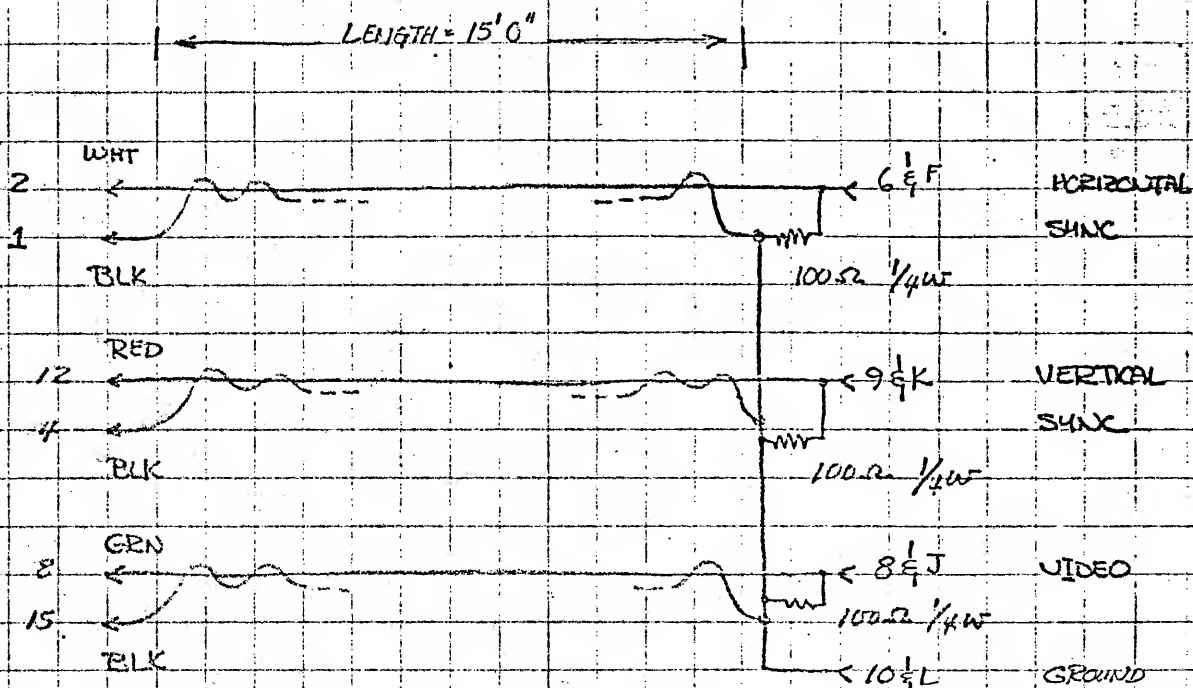
DISPLAY EXTERNAL CABLE

2 OF 1

4-15-74 CT

ALTO END

MONITOR END



CANNON

CABLE:

AMPHENOL

QTY

PART:

BELDEN # 9745

#225-21031-101

(1) DAC-15P SHELL

CONNECTOR

(1) DA 51210-1 PLASTIC JUNCTION SHELL

(6) 030-1952-000 PINS

(1) DA 51220-1 SLIDING LOCK RETAINER

1 REQD / SYSTEM

PIN INSERTION/EXTRACTION TOOL: CIST 20HDB

CRIMP TOOL M22520/9-PL

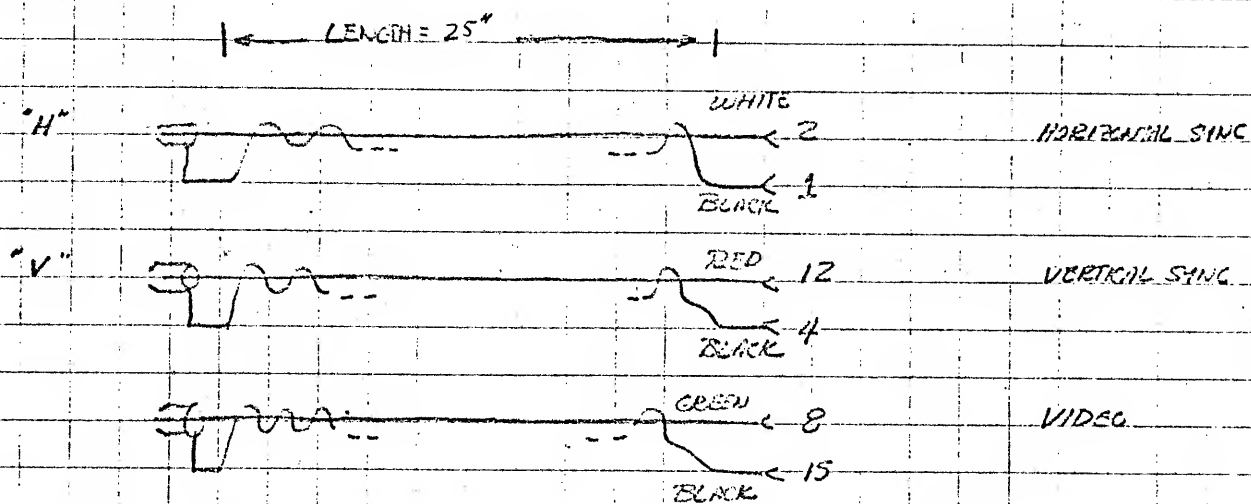
LOCATOR TH185

ALTO

DISPLIN INTERNAL CABLE

1 OF 1

4-15-74 CT



CABLE:

BELDEN #9745

↑  
CANNON

DAC 153 SHELL

(3) AMP 20197-3 CONNECTOR PIN

(6) 030-1953-000 FEMALE CONTACT

(3) AMP 329006 FERRULE

CRIMP TOOL IS AMP #45634-3

1 REQD/SYSTEM

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
TERMINATOR +5	A/ 1		B/ PP	
GROUND	59		D	} THESE PINS ARE COMMON ON THE PADDLEBOARD
GROUND	60		DD	
GROUND	61		WW	
DISK'	67		R	
DISK	69		L	
CYL(7)'	73		N	
SKINC'	74		TT	
RDCLK'	76		A	
READY'	78		U	
RESTOR'	79		VV	
KSECT(3)	80		CC	
CYL(3)'	81		FF	
WRTGATE'	82		EE	
SRWRTDY'	83		F	
KSECT(1)	84		KK	
KSECT(2)	85		JJ	
CYL(8)'	86		LL	
RDDATA'	87		C	
CYL(4)'	88		X	
CYL(1)'	89		BB	
CYL(5)'	90		J	
WRTDATA'	91		B	
CYL(6)'	93		RR	
HEAD'	94		AA	
STROBE'	96		SS	
SECT(4)'	100		W	
RDGATE'	103		E	
LAI'	104		XX	
ADRACK'	105		NN	



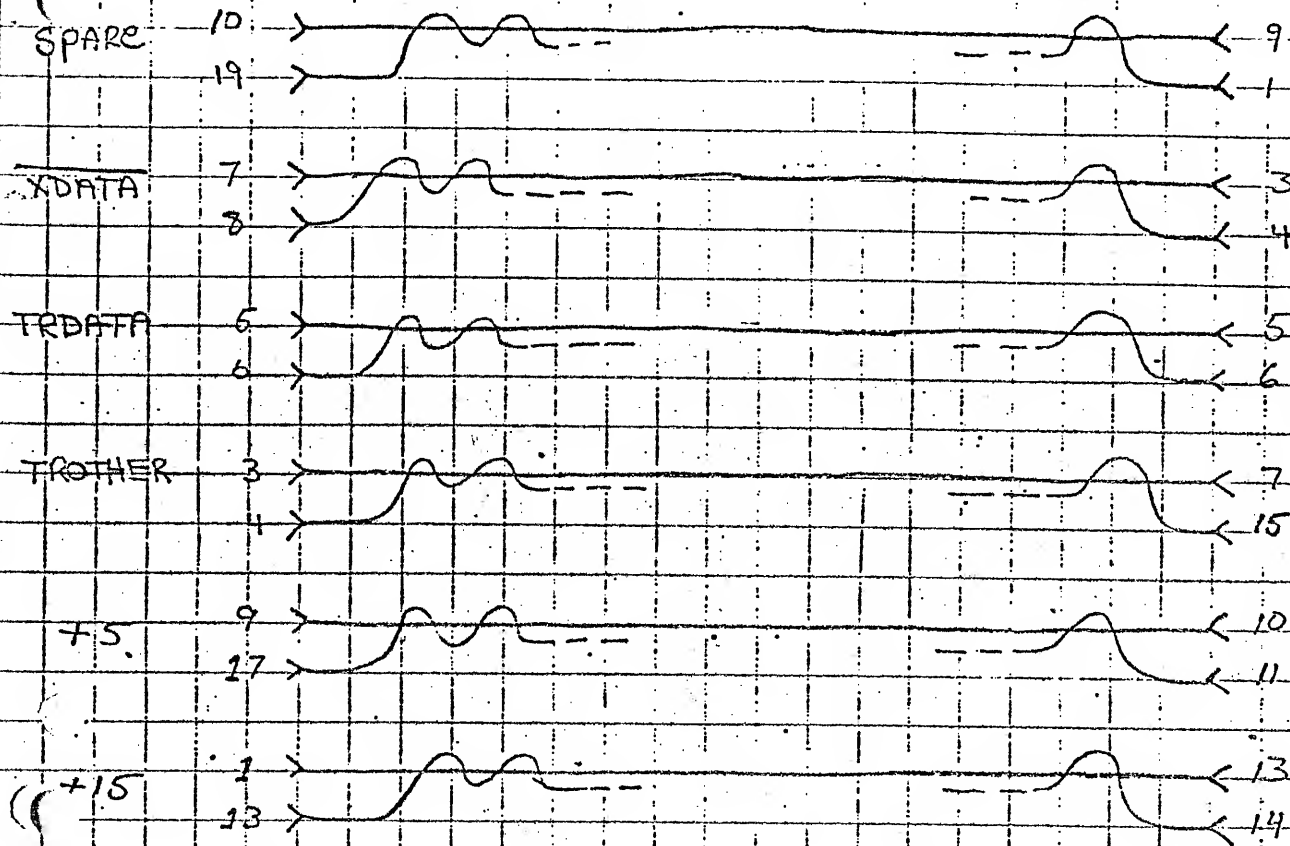
SIGNAL NAME	ALTO BUS INFORMATION	Alto 1 37 PIN CANNON	Alto 2 25 PIN CANNON	WIRE COLOR
-PPFSTR	BUSOUT(00)	1	13	
-PREST	BUSOUT(01)	2	25	
-PRIB	BUSOUT(02)	3	12	
-PCHSTR	BUSOUT(03)	4	24	
-PCARSTR	BUSOUT(04)	5	11	
-PDATA1024	BUSOUT(05)	6	23	
-PDATA512	BUSOUT(06)	7	10	
-PDATA256	BUSOUT(07)	8	22	
-PDATA128	BUSOUT(08)	9	9	
-PDATA64	BUSOUT(09)	10	21	
-PDATA32	BUSOUT(10)	11	8	
-PDATA16	BUSOUT(11)	12	20	
-PDATA8	BUSOUT(12)	13	7	
-PDATA4	BUSOUT(13)	14	19	
-PDATA2	BUSOUT(14)	15	6	
-PDATA1	BUSOUT(15)	16	18	
-PPFRDY	BUSIN(00)	17	5	
-PCHK	BUSIN(01)	20	17	
-PPO	BUSIN(02)	21	4	
-PCHRDY	BUSIN(03)	22	16	
-PCARRDY	BUSIN(04)	23	15	
-PRDY	BUSIN(05)	24	3	
PRINTERGND	LOGICGND	25	14	
PRINTERGND	LOGICGND	26	1	
PRINTERGND	LOGICGND	27		
PRINTERGND	LOGICGND	28		
PRINTERGND	LOGICGND	29		
POWERGND	LOGICGND	18		
PRINTER+15V	+15V	19		
PRINTER-15V	-15V	36		
PRINTER+5V	VCC	37		

# ETHERNET INTERNAL CABLE 1 of 1

6/26/79 DB

Length 26"

1 to 1 for ATO I



AMP

CABLE: BELDEN 8747

CANNON

QTY	PART
(1)	87133-6 SHELL
(10)	87165-1 Pins

QTY	PART
(1)	DAC 15S SHELL
(10)	030-1953-000 Female CONTACT

CRIMP TOOL IS AMP 90289-1  
EXTRACTION TOOL IS AMP 91084-1

(2) D53018 SLIDING LOCK P

1 Required / system

20	10
19	9
18	8
17	7
16	6
15	5
14	4
13	3
12	2
11	1

PIN numbering FOR AMP CONNECTOR - CABLE END SHOWN.

NOTE that the socket is NOT Keyed. which ever way you position it IS OK.